MICROSYSTEMS FOR REAL-TIME NEUROCHEMICAL MONITORING USING FAST-SCAN CYCLIC VOLTAMMETRY

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MICROSYSTEMS FOR REAL-TIME NEUROCHEMICAL MONITORING USING FAST-SCAN CYCLIC VOLTAMMETRY

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Dopamine is an important neurotransmitter that plays a fundamental role in motor control and reward-seeking behaviors. Electrochemical detection of dopamine is accomplished through fast-scan cyclic voltammetry (FSCV), a neurochemical monitoring technique that can resolve rapid changes in dopamine concentration with subsecond temporal resolution and high selectivity. This dissertation describes the development of several microsystems for real-time monitoring of dopamine levels using FSCV, including a wide-range analog-to-digital converter (ADC), a fully-integrated low-power wireless sensing system, and a scalable electrochemical detector array. The work described here tackles some of the challenges that exist in the field of neuroscience to advance two important applications: long-term *in vivo* monitoring in freely-behaving animals using carbon-fiber microelectrodes (CFMs) and high-throughput drug screening using planar microelectrode arrays (MEAs).

In particular, a low-power two-step cyclic ADC for wide-range acquisition of neurochemical signals is demonstrated. The system was validated by recording flow-injection of 2-μM dopamine at a CFM using 300-V/s FSCV. A 30-μW wireless microsystem for real-time *in vivo* monitoring and a lightweight miniaturized device that can enable long-term behavioral studies in freely-behaving animals are also demonstrated. On-chip integration of analog background subtraction and UWB telemetry yields a 32-fold increase in resolution versus stan-

dard Nyquist-rate conversion alone, near a four-fold decrease in the volume of uplink data versus single-bit, third-order, delta-sigma modulation, and more than a 20-fold reduction in transmit power versus narrowband transmission at low data rates. The system was validated by wirelessly recording flow-injection of dopamine with concentrations in the range of 250 nM to 2 μM at a CFM using 300-V/s FSCV. Measurement results indicate an input-referred current noise of 92 pA_{rms} and an input current range of ±430 nA at a conversion rate of 10 kHz. A scalable 32 × 32 (1,024-electrode) CMOS VLSI potentiostat array for high-throughput drug screening applications is also presented. The core of the array is a high-precision bidirectional-current detector that enables both amperometry and FSCV using MEAs for massively-parallel detection of transmitter release as well as electrode impedance characterization.

BIOGRAPHICAL SKETCH

Carlos Iván Dorta Quiñones was born and raised in Puerto Rico. He received the B.S. degree in electrical engineering and computer science from Massachusetts Institute of Technology (MIT), Cambridge, MA, in 2004 and the M.S. degree in electrical engineering from Boston University, Boston, MA, in 2007. He joined the Ph.D. program in electrical and computer engineering at Cornell University, Ithaca, NY in 2007.

During his graduate studies, he held internships at Mitsubishi Electric Research Laboratories, Freescale Semiconductor, and IBM. His research interests include low-power analog, mixed-signal, and radio-frequency integrated circuit design for biomedical applications.

A mis padres, Paulino Dorta Pérez y Cynthia E. Quiñones Morales,

y a mi esposa, Gretchen Ruethling,

por todo su amor y apoyo.

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I was introduced to Cornell University when I participated in a pre-college summer program as a high school junior at the encouragement of one of my teachers. Little did I know at the time what a pivotal experience in my life it would be. Before that, I had never considered pursuing higher education outside my little island of Puerto Rico. Cornell's Summer College opened my eyes to the great educational opportunities that were out there and sparked my interest in subsequently studying electrical engineering at MIT. Now, a decade and a half after my introduction to Cornell, I find myself at the end of a long journey, completing my doctoral studies. I want to express my gratitude to the many people who were instrumental in my success in this endeavor.

First, I thank my advisors, Professors Alyssa Apsel and Manfred Lindau, for the opportunity to pursue an interdisciplinary research project at the intersection of nanotechnology and neuroscience, and for their guidance, patience, and support. I am also grateful to Professor Alyosha Molnar for reading and providing feedback on my thesis, Professor Bradley Minch, from Olin College, for his collaboration, and Scott Coldren for his help with all the paperwork. I am enormously thankful to my colleagues and mentors Xiao Wang and Rajeev Dokania, who always had time for my questions and provided me with valuable input without which this work would have not been possible. Many thanks to Alycia Gailey and Brian Kim for their knowledge and advice, and to Joan Lenz for her flawless technical expertise. I am also grateful to all colleagues in the Apsel and Lindau research groups for their friendship and support.

I am deeply indebted to all of my friends and family who made my Ph.D. experience memorable and enjoyable. I thank Scott MacDonald and Erica Ostermann for creating a warm community and giving me the opportunity to serve

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LIST OF ABBREVIATIONS

ΣΔ	Sigma-Delta
A/D	Analog-to-Digital
ADC	A/D Converter
BER	Bit Error Rate
CDS	Correlated Double Sampling
CFM	Carbon Fiber Microelectrode
CMOS	Complementary MOS
DA	Dopamine
DAC	Digital-to-Analog Converter
FCC	Federal Communications Commission
FSCV	Fast-Scan Cyclic Voltammetry
IC	Integrated Circuit
IR	Impulse Radio
I/V	Current-to-Voltage
LSB	Least Significant Bit
MEA	Micro-Electrode Array
MDAC	Multiplying DAC
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
OOK	On-Off Keying
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
RCA	Regulated Cascode Amplifier
RCG	Regulated Common Gate
RE	Recording Electrode
RX	Receiver
SAR	Successive Approximation Register
S/H	Sample and Hold
SRAM	Static Random Access Memory
TIA	Transimpedance Amplifier
TX	Transmitter
UWB	Ultra-Wideband
VCO	Voltage-Controlled Oscillator
VLSI	Very Large Scale Integration
WE	Working Electrode

CHAPTER 1
INTRODUCTION

1.1 Motivation

A long-standing goal of neuroscience has been to understand the neural basis of brain function and behavior. Monitoring neurotransmitter release in small animals and in living cells is one approach neuroscientists have used to elucidate the underlying mechanisms of neuronal communication and to develop treatments that modulate these mechanisms. Dopamine is an important neurotransmitter that has been the subject of active research because it plays a fundamental role in motor control, motivation, pleasure, social behavior, and reward-based learning [4, 11, 23]. Real-time electrochemical detection of extracellular dopamine levels is accomplished through fast-scan cyclic voltammetry (FSCV), a neurochemical monitoring technique capable of resolving rapid changes in dopamine concentration with subsecond temporal resolution and high selectivity. This dissertation describes the development and validation of several microsystems for neurochemical monitoring of dopamine levels using FSCV, including a wide-range analog-to-digital converter (ADC), a fully-integrated low-power wireless sensing system, and a scalable electrochemical sensor array. Together, the work described here addresses and solves some of the existing challenges in the field of neuroscience to enable two important applications: long-term *in vivo* monitoring studies in freely-behaving animals using a carbon-fiber microelectrode (CFM) and high-throughput drug screening using a planar microelectrode array (MEA).

1.2 Background

1.2.1 Neurotransmitter Release

Neurons communicate with each other via chemical messengers called neurotransmitters, which are stored in membrane-bound secretory vesicles attached to the inside of the plasma membrane of the presynaptic terminal [46]. When the terminal is electrically stimulated via an action potential, the secretory vesicles fuse with the plasma membrane to release the neurotransmitter molecules into extracellular space [33]. The secreted neurotransmitters then bind onto receptors on the post-synaptic terminal, causing the generation of another action potential and thus, effectively transmitting information between neurons. Transmitter release has been the focus of much attention in the field of neuroscience because of its intricate relationship to brain function and behavior.

1.2.2 Dopamine

There are many kinds of neurotransmitters in the brain, but this dissertation focuses specifically on dopamine, which is of great interest to neuroscientists due to the important role it plays in motor control, social behavior, motivation, pleasure, and reward-based learning [4, 11, 23]. The disruption of dopamine systems in the brain leads to brain disorders and diseases such as Parkinson's, schizophrenia, depression, and drug abuse [18]. Real-time electrochemical detection of dopamine is essential for neuroscientists to elucidate the underlying causes of these disruptions and to develop treatments that regulate these dopamine systems.

1.2.3 Recording Techniques

Over the past few decades, two recording techniques that have become the most prevalent for monitoring neurotransmitter release: amperometry [10, 49] and FSCV [5, 50] at a polarizable working electrode. In amperometry, a constant potential is applied to the working electrode. Dopamine molecules secreted during neurotransmitter release oxidize when they come into contact with the surface of the electrode, losing two electrons each in the process, and thus creating a small transient current [16]. However, any other electroactive species that oxidize below the applied voltage will also contribute to the total current. Thus, this technique does not allow the identification of the released compounds. FSCV overcomes this limitation through the use of a linear voltage ramp instead of a constant potential. In FSCV, the voltage applied to the electrode is ramped linearly with time. Dopamine molecules oxidize at around +0.6 volts, creating a small positive oxidation current when the ramp reaches this voltage. Because different molecules oxidize at different voltages, any other electroactive compounds present will oxidize at different times. Thus, FSCV allows for identification and discrimination of the released compounds.

1.2.4 Microelectrodes

As mentioned previously, this dissertation focuses on two neuroscience applications: *in vivo* monitoring and drug screening. Traditionally, a CFM has been used as the working electrode due its chemically inert properties, small dimensions, i.e., ~5–20 μm diameter, and thus fast response time [22]. Because a CFM is also biocompatible, it has typically been the sensor of choice for *in vivo* mon-

itoring applications. However, experiments with a CFM are typically limited to single-unit recordings because each experiment is time-consuming and laborious, requiring precise manual positioning of the CFM under microscopic observation. Although a CFM is adequate for single-unit *in vivo* monitoring, it is not suitable for drug screening, a process that requires a statistically significant set of measurements to obtain conclusive evidence on the effect of a drug on transmitter release. Thus, in high-throughput screening the traditional CFM has been replaced with a planar MEA, which can be batch fabricated with high reproducibility [52, 53], to measure neurotransmitter release from a large number of cells in parallel and thus accelerate the development of treatments that modulate transmitter release. Surface-patterned planar MEAs using noble metals such as gold and platinum have recently been applied to measure quantal release events from single cells [2, 6, 24, 51]. Amperommetry and FSCV using MEAs have recently been demonstrated in [34, 54]. Amperometry using MEAs allows the simultaneous recording of quantal release events from a large number of cells. FSCV using MEAs serves as a complimentary technique that allows the simultaneous identification of multiple secreted compounds across different types of cells [26]. The latter technique is also useful to perform batch impedance characterization of surface-patterned electrodes by comparing voltammograms obtained using a redox reporter biomolecule against a known standard [17].

1.3 Organization

This dissertation is organized as follows: Chapters 2 and 3 will focus on the design of novel circuits that can enable long-term *in vivo* monitoring studies.

Chapter 2 describes a technique that increases the resolution of the ADC and simultaneously reduces the data rate of the wireless link in integrated wireless monitoring systems, and also describes a two-step cyclic ADC architecture that implements the proposed scheme. Chapter 3 describes a low-power wireless microsystem that uses the ADC described in Chapter 2 with additional low-power analog sensing and wireless transmitter blocks to enable long-term monitoring studies in freely-behaving animals. Chapter 4 will focus on a scalable electrochemical detector array that can enable high throughput drug screening. The core of the array is a potentiostat circuit that can measure bidirectional currents with high precision, thus enabling fast scan cyclic voltammetry.

1.4 Acknowledgements

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CHAPTER 2

A TWO-STEP CYCLIC A/D CONVERTER WITH WIDE DYNAMIC RANGE FOR REAL-TIME NEUROCHEMICAL MONITORING USING FAST-SCAN CYCLIC VOLTAMMETRY

2.1 Introduction

Real-time electrochemical detection of cerebral dopamine is essential for neuroscientists to elucidate the underlying mechanisms of behavioral and pharmacological events, such as reward-based learning, social interaction, and therapeutic regulation of neurodegenerative diseases like Parkinson's disease, in awake animals [40]. Real-time, *in vivo* monitoring of dopamine is typically achieved through fast-scan cyclic voltammetry (FSCV), a leading electrochemical technique that can resolve the concentrations of multiple electroactive species in time scales much smaller than the time course of neurotransmitter fluctuations in the mammalian brain [39].

The levels of precision required to detect dopamine-induced fluctuations, which are orders-of-magnitude smaller than the background transients elicited in FSCV, mandate high-resolution acquisition systems, typically accompanied by hardwired setups with a cable tether linking the animal to the recording equipment [20]. The cable tether imposes a significant amount of stress on the animal which can lead to artifacts in the recording, and restricts the animal's movement, limiting the types of experiments that can be performed. Several approaches have circumvented these drawbacks by using *in vivo* telemetry instead [20,32,35]. However, these wireless setups are still implemented with discrete components which consume signifiant power and area. Recent integrated

wireless designs have addressed these concerns, achieving low-power, stress-free monitoring at the expense of resolutions much lower than those obtained with the high-performance discrete-component implementations [42].

This chapter describes a low-power, on-chip dynamic range enhancement technique for integrated neurochemical monitoring systems. Dynamic analog background subtraction techniques have been shown to reduce the quantization error of the analog-to-digital converter (ADC) block in these systems [27]. The proposed scheme uses a similar approach with a superior error correction technique to enable on-chip integration of low-power, moderate-resolution ADC topologies with a performance equivalent to their high-resolution counterparts. As a proof of concept, a novel two-step cyclic ADC architecture that implements the proposed scheme is presented.

2.2 FSCV Theory

In a typical FSCV experiment, a 10-ms triangle wave is applied to a working electrode, such as a carbon fiber microelectrode (CFM), at a rate of ~300 V/s from a baseline potential of −0.4 V up to a peak potential of +1.0 V and back down to −0.4 V, as illustrated in Figure 2.1. At the onset of the scan, different electroactive species present in the brain tissue begin to oxidize as the potential increases. Dopamine molecules oxidize around +0.6 V, losing two electrons each, and therefore produce a small *faradaic* current. As the various electroactive species present in the tissue continue oxidizing with increasing potential, an increasing number of ions starts to drift, charging the electrode capacitance, and in turn, producing large background transient currents that essentially bury

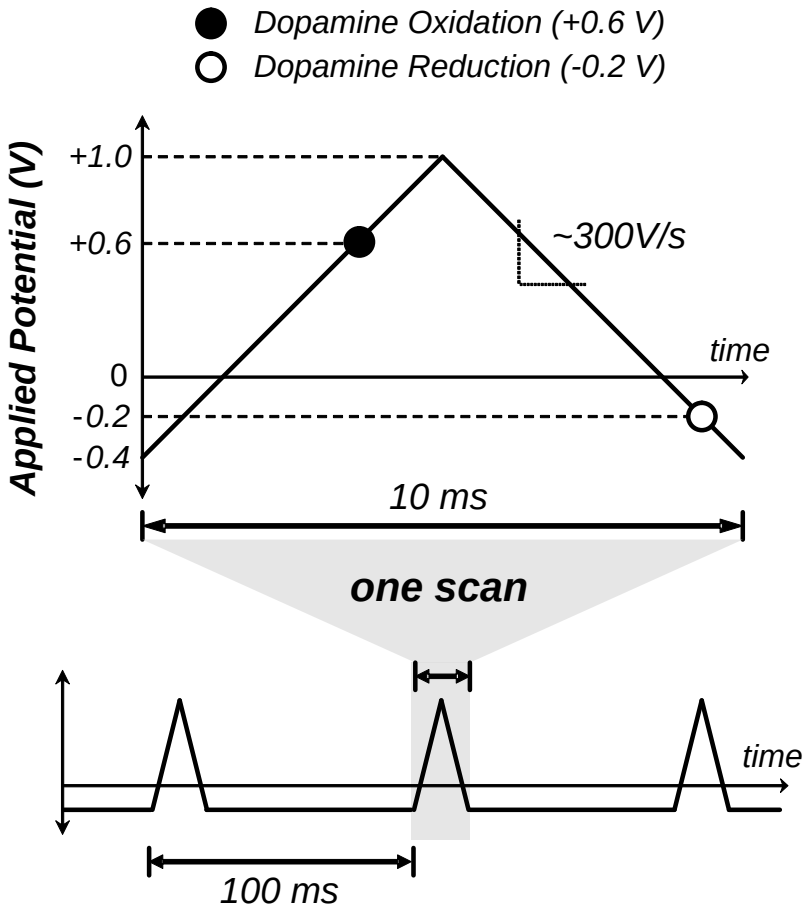

Figure 2.1: Electrochemical detection of dopamine using fast-scan cyclic voltammetry (FSCV) at a carbon-fiber microelectrode (CFM). A 10-ms, 300-V/s triangle waveform is applied to the CFM every 100 ms. Dopamine oxidation and reduction occurs near +0.6 V and −0.2 V, respectively.

the small dopamine-induced *faradaic* currents. Similar background transients of opposite magnitude occur in the negative phase of the scan, during reduction of the electroactive species. A transimpedance amplifier (TIA) converts the net current elicited in each scan into a voltage that is then digitized for offline post-processing. To obtain the temporal pattern of changes in dopamine concentration, consecutive scans are repeated at an interval of 100 ms. During post-processing, the average of a set of background transients elicited just before dopamine release is subtracted from the transients elicited during dopamine detection, yielding

$$v_{out} = v_{DA} - v_{bkg}, \tag{2.1}$$

where v_{DA} and v_{bkg} are the voltages at the output of the TIA that are proportional to the dopamine-induced and background transients illustrated in Figure 2.2(a), and v_{out} is background-subtracted voltammetric output of interest proportional to the *faradaic* output current illustrated in Figure 2.2(b).

2.3 Principle of Operation

Figure 2.3 illustrates the proposed two-step acquisition scheme. The scheme takes advantage of the temporal stability of the background currents [39, 40] to improve the dynamic range of the system by performing real-time background subtraction in a two-step manner before acquisition of the voltammetric output. In the first step, ϕ_1, a copy of an initial background transient is stored in memory and synthesized in synchrony with a subsequent background transient to compute the quantization error in the approximation of the background. In the

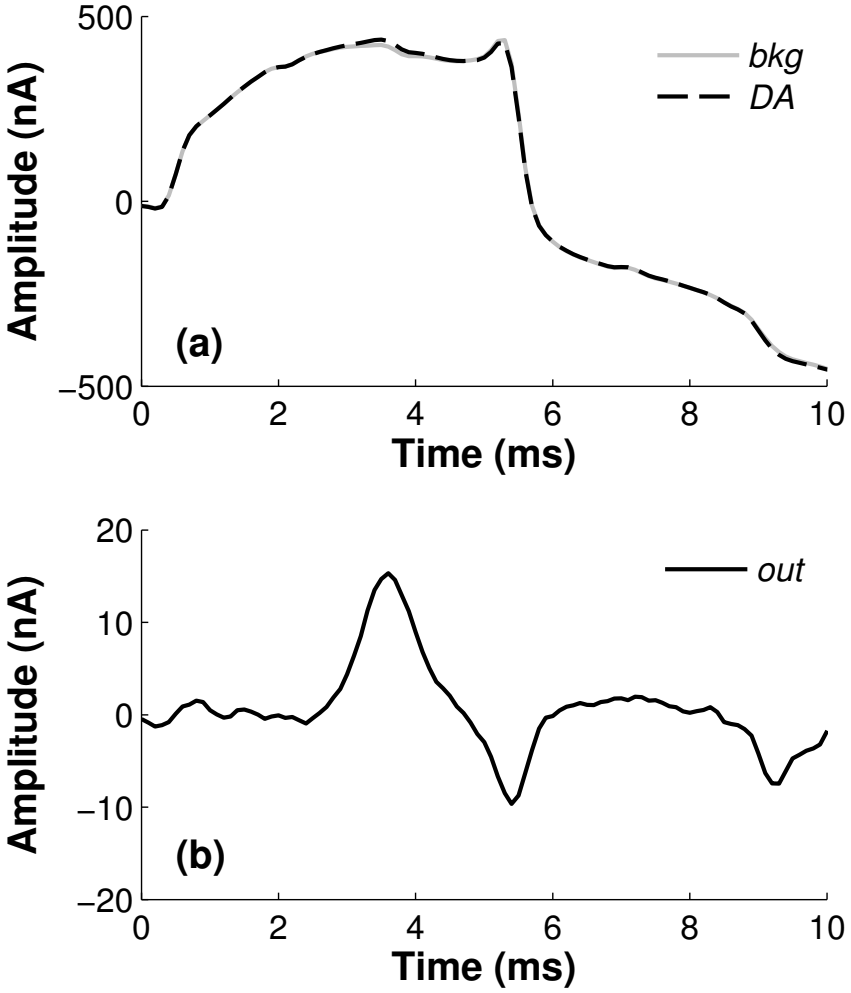

Figure 2.2: (a) Typical background (*bkg*) and dopamine-induced (*DA*) transient currents produced in a single FSCV scan. (b) Background-subtracted *faradaic* current output (*out*).

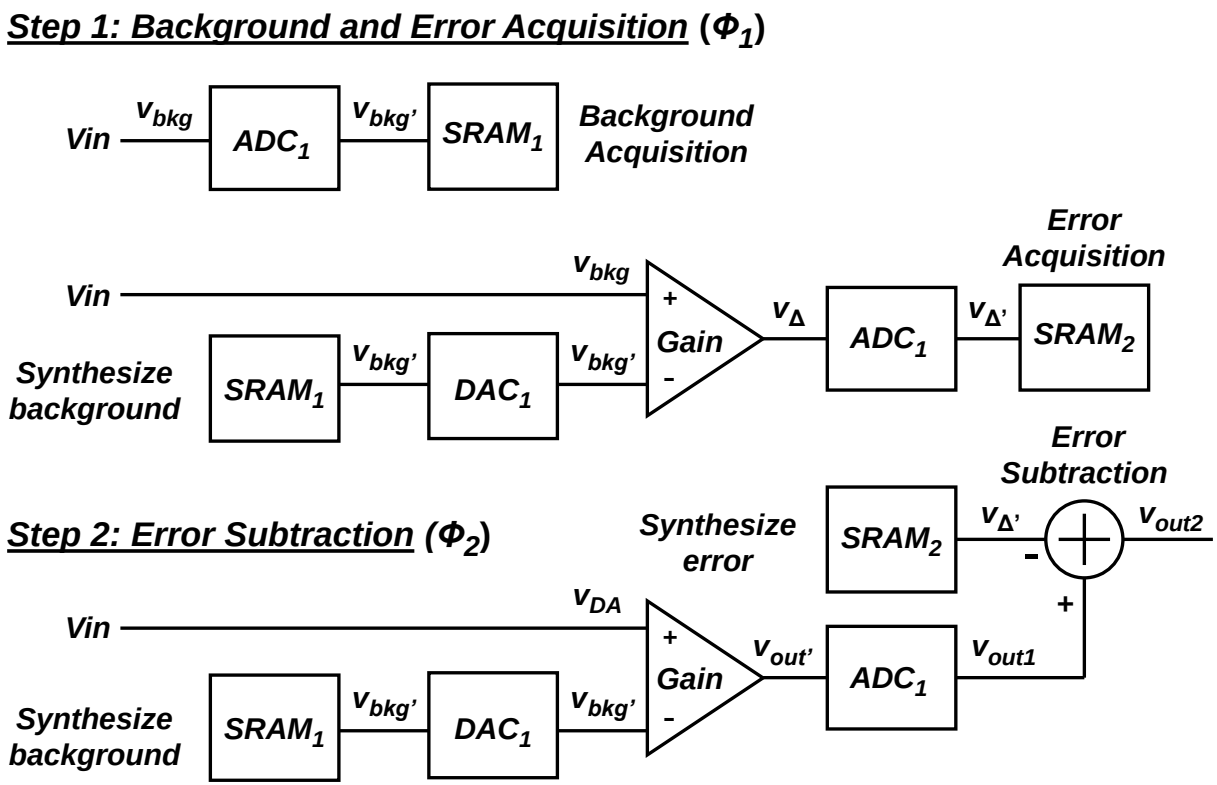

Figure 2.3: Proposed two-step signal acquisition scheme.

second step, ϕ_2, the same background copy is synthesized again, this time in synchrony with a dopamine-induced transient, to compute an estimate of the voltammetric output. By subtracting amplified versions of the error computed in ϕ_1 from the estimate computed in ϕ_2, the effective resolution of the system is significantly enhanced.

Because the proposed acquisition system is intended for integrated monitoring systems, background subtraction is done in discrete-time to avoid the use of the external reconstruction filters. Due to the discrete nature of the scheme, the following shorthand notation will be used to represent the i^{th} sample of any continuous- or discrete-valued discrete-time signal, v_X, where

$$\left\{\forall i \in \mathbb{Z}^+ \;\middle|\; i \leq M\right\}, v_x(t)\big|_{t=i\cdot T_s} = v_x[i] = v_{x_i}, \tag{2.2}$$

for any M samples acquired with sampling period T_S. For simplicity, the subscript i in Equation 2.2 will be dropped in the ensuing analysis.

2.3.1 Background and Error Acquisition

The first step, ϕ_1, is performed during baseline levels of cerebral dopamine, in which FSCV scans elicit background transients (Figure 2.2(a)). At the onset of some initial scan, ϕ_{1a}, v_{bkg} is digitized via ADC_1, and stored in memory $SRAM_1$, yielding

$$v'_{bkg} = v_{bkg} - v_\Delta, \quad v_\Delta \in [0, V_{LSB}], \tag{2.3}$$

where v'_{bkg} is the resulting background copy, and v_Δ is the residue of the conver-

sion. At the onset of the next scan, ϕ_{1b}, v'_{bkg} is synthesized via DAC_1 in synchrony with v_{bkg}. The residue, $v_\Delta = v_{bkg} - v'_{bkg}$, is amplified by fixed gain A, digitized via ADC_1, and stored in memory $SRAM_2$, yielding

$$v'_\Delta = v_\Delta - \frac{v_{\Delta_1}}{A}, \quad v_{\Delta_1} \in [0, V_{LSB}], \tag{2.4}$$

where v_Δ is the effective residue after gain normalization, and v_{Δ_1} is the residue from conversion of the amplified residue.

2.3.2 Error Subtraction

The second step, ϕ_2, is performed during dopamine release, in which FSCV scans elicit dopamine-induced transients (Figure 2.2(a)). At the onset of each consecutive FSCV scan, v'_{bkg} is reproduced via DAC_1 in synchrony with v_{DA}. From Equation 2.1 and Equation 2.3, the difference $v'_{out} = v_{DA} - v'_{bkg}$ is also amplified by gain A and digitized via ADC_1, yielding

$$v_{out_1} = v'_{out} - \frac{v_{\Delta_2}}{A} = v_{out} + v_\Delta - \frac{v_{\Delta_2}}{A}, \quad v_{\Delta_2} \in [0, V_{LSB}], \tag{2.5}$$

where v_{out_1} is the effective output after gain normalization, and v_{Δ_2} is the residue from conversion of the amplified output. Real-time binary subtraction of Equation 2.4 from Equation 2.5 further improves the precision of the acquired output, yielding

$$v_{out_2} = v_{out} - \frac{v_{\Delta_2} - v_{\Delta_1}}{A}, \quad \{v_{\Delta_2} - v_{\Delta_1}\} \in [-V_{LSB}, V_{LSB}], \tag{2.6}$$

where v_{out_2} is the effective voltammetric output after gain normalization.

2.4 System Analysis

2.4.1 Gain Requirement

The ideal gain requirement for full scale amplification of the voltammetric output is given by

$$A_0 \cdot v_{out-\mathrm{pp}} = V_{FS} \Rightarrow A_0 = \frac{1}{k}, \quad k = \frac{v_{out-\mathrm{pp}}}{V_{FS}}, \tag{2.7}$$

where A_0 is the ideal gain required for full scale amplification, $v_{out-\mathrm{pp}}$ is the swing of the voltammetric output, V_{FS} is the full scale voltage, and k is the voltammetric swing normalized to full scale. From Equation 2.7, it is evident that the gain requirement increases drastically with decreasing swing. For small output swings, the large gains required essentially mitigate the effect of the residue v_{Δ_2} in Equation 2.5, yielding

$$A \cdot v'_{out-\mathrm{pp}} = V_{FS} \Rightarrow A = A_0 \left(1 + \frac{v_{\Delta-\mathrm{pp}}}{v_{out-\mathrm{pp}}}\right)^{-1}, \quad v_{\Delta-\mathrm{pp}} \in [-V_{LSB}, V_{LSB}], \tag{2.8}$$

where A is the actual gain required, $v_{out-\mathrm{pp}}$ is the difference between the two voltammetric samples having maximum and minimum amplitude among all M samples, and $v_{\Delta-\mathrm{pp}}$ is the difference between the respective residues from conversion of each of these two samples. From Equation 2.8, $v_{\Delta-\mathrm{pp}}$ is continuous-valued over $\pm V_{LSB}$, and for a given normalized swing k, sets the gain requirement. Choosing $v_{\Delta-\mathrm{pp}} = +V_{LSB}$ in Equation 2.8 as worst-case yields the least amplification but ensures that none of the amplified output samples clip for a given swing. Using this value along with Equation 2.7, the required gain becomes a function of normalized swing k and resolution N of the ADC, yielding

$$A = A_0 \left(1 + \frac{1}{k \cdot 2^N}\right)^{-1}. \tag{2.9}$$

2.4.2 Dynamic Range Enhancement

The effective resolution is given by

$$R = \log_2 \left(\frac{A \cdot v_{out-\text{pp}}}{\max |v_{error}|}\right), \tag{2.10}$$

$$v_{error} = \frac{v_{\Delta_2} - v_{\Delta_1}}{A}, \quad v_{error} \in \left[-\frac{V_{LSB}}{A}, \frac{V_{LSB}}{A}\right], \tag{2.11}$$

where R is the total effective resolution, in bits, and v_{error} is the effective residue of the error-corrected output in Equation 2.6. This residue is continuous-valued over $\pm\frac{V_{LSB}}{A}$, exhibiting a worst-case magnitude of $\frac{V_{LSB}}{A}$. Plugging the latter value in Equation 2.10 for the maximum absolute error, and using Equation 2.5 and Equation 2.9 yields

$$R = \log_2 \left[A \cdot \left(2^N - A\right)\right] \approx N + \log_2(A), \tag{2.12}$$

for a total dynamic range enhancement of $\log_2(A)$ for large values of N.

2.5 Simulation-Based Studies

The theoretical gain requirement and dynamic range enhancement of the system were initially analyzed. Figure 2.4 illustrates the required gain as well as

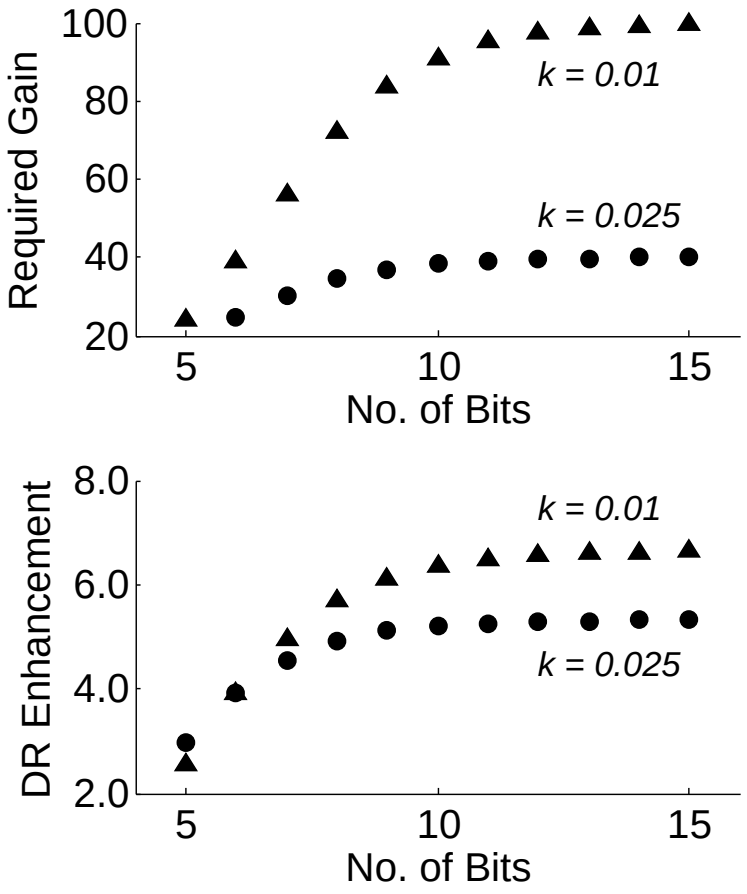

Figure 2.4: (a) Gain requirement and dynamic range enhancement (in bits) vs. normalized voltammetric swing k and ADC resolution N.

the additional bits gained, i.e., dynamic range enhancement, with the proposed scheme as a function of normalized voltammetric swing k and ADC resolution N. As both sets of curves exhibit a point of diminishing return above 9–10 bits, a 9-bit SAR-ADC topology was chosen as an optimum to ensure a low-cost, low-power design. For a resolution of 9 bits, effective dynamic range enhancements of 5.0 and 6.0 bits were calculated for normalized voltammetric swings of 2.5% and 1% full scale, respectively, as seen in Figure 2.4.

Behavioral models of the circuit blocks in Figure 2.3 were implemented in Verilog-A and a simulation was performed with the currents shown in Figure 2.2(a) serving as inputs to the system (after ideal signal transduction with a gain of 1 V/μA and an offset of 0.5 V). Figure 2.5 shows the amplified voltammetric output (Fig. 2.5(a)) corresponding to the *faradaic* signal in Figure 2.2(b), and effective residues obtained from conversion with an ideal 14-bit ADC (Fig. 2.5(b)) as well as with the proposed scheme (Fig. 2.5(c)). Simulation results yielded an output swing of 932.8 mV for the amplified voltammetric output, $A \cdot v_{out-\mathrm{pp}}$, and a peak absolute residue, $\max|v_{error}|$, of 53.0 μV. Another benchmark simulation, performed with an ideal 14-bit ADC, yielded a peak absolute residue of 58.7 μV. A voltammetric signal with a swing of 2.5% full scale, and a differential amplifier with a gain of 35 were used in both simulations. The output DC level of the amplifier was designed to yield maximal amplification without clipping. Plugging the results above into Equation 2.10 yielded effective resolutions of 14.0 and 14.1 bits, respectively, for the ideal 14-bit ADC and the proposed conversion scheme, in close agreement with the theoretical predictions. Effective number of bits (ENOB) figures of 13.4 and 12.9 bits were also found for the ideal 14-bit ADC and the proposed conversion scheme, respectively, using the RMS values of the signals in Figure 2.5.

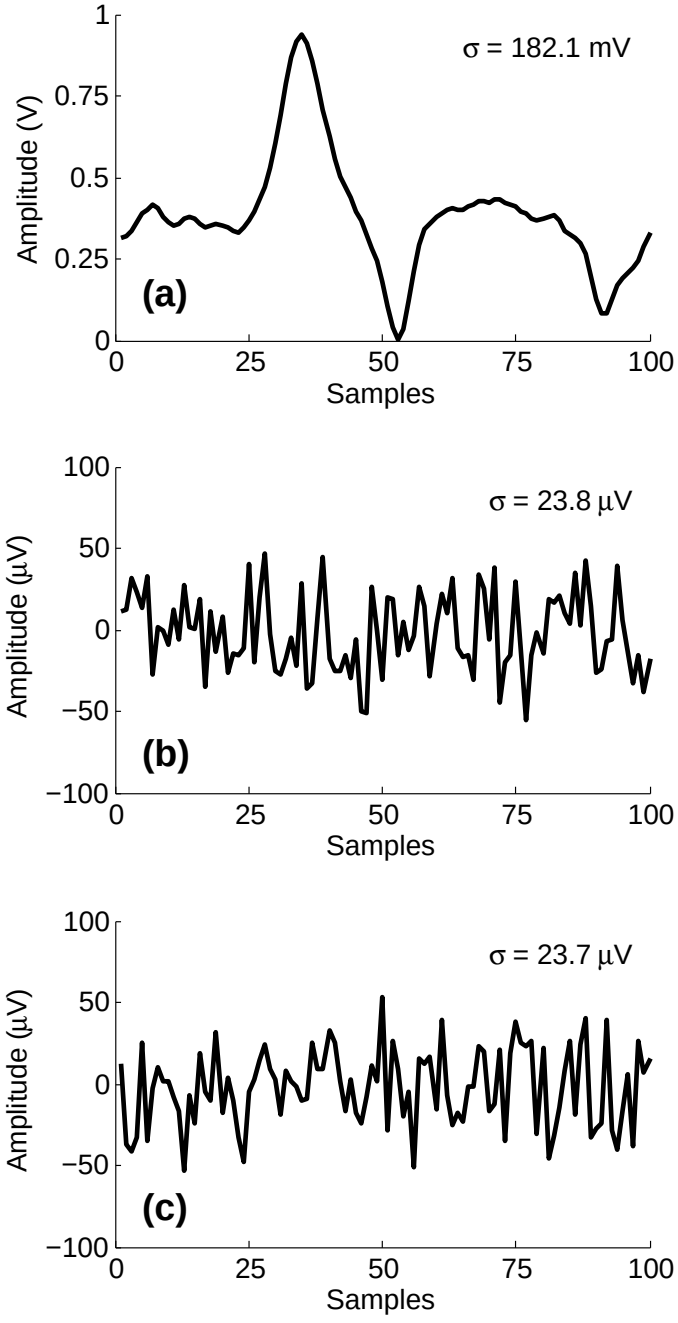

Figure 2.5: (a) Simulated voltammetric output proportional to the *faradaic* signal in Fig. 2.2(b). Total quantization error from (b) an ideal 14-bit conversion and (c) the proposed two-step conversion.

2.6 Circuit Implementation

A two-step cyclic ADC, based on the circuit blocks shown in Figure 2.3, was designed and implemented in a TSMC 65-nm process as a proof of concept. Figure 2.6 shows the architecture of the core ADC, comprised of a 9-bit successive-approximation-register (SAR) ADC, a 9-bit multiplying digital-to-analog converter (MDAC) and two 100 × 9-bit, 6T-SRAM modules with their corresponding timing logic. Figure 2.7 shows the timing diagram of the core ADC.

2.6.1 Successive Approximation ADC

Operation of the 9-bit SAR-ADC shown in Figure 2.8 is similar to that described in [31]. Bits are resolved using offset binary encoding to avoid the use of noisy charge pumps and enable low-power operation from a 1.2-V supply. References V_{REF+} and V_{REF-} are set to 1.2 V and 0 V, respectively, yielding a full scale that spans the entire supply range. The binary-weighted capacitor array of the SAR-ADC is laid out in a 1-D common-centroid geometry with a unit capacitance value of 62.5 fF for kT/C noise considerations as well as to mitigate offset and gain errors due to capacitor mismatch and charge injection.

Control Logic

Bit cycling is achieved through a 10-digit Johnson counter. At the rising edge of a 10-μs clock, CLK, the counter increases its count, shifting through its decoded outputs in a sequential manner. In the first bit cycle, $C0$, the comparator is auto-zeroed (AZ) and the bottom plates of the capacitor array sample the input v_{IN}. In

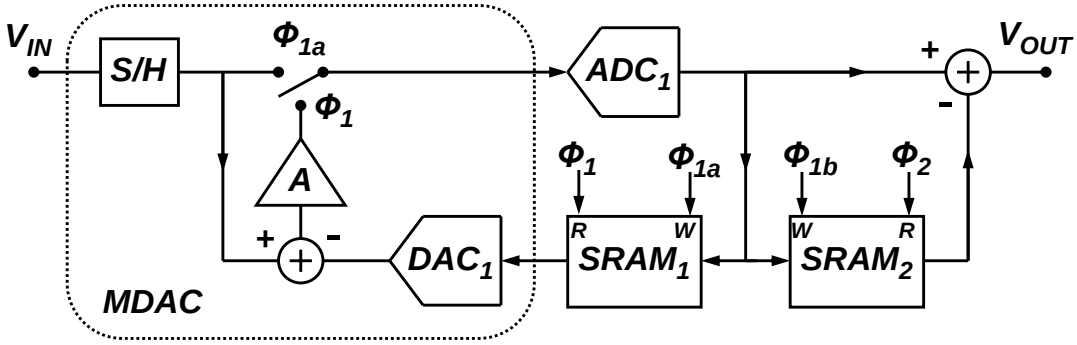

Figure 2.6: Block diagram of the proposed two-step A/D converter.

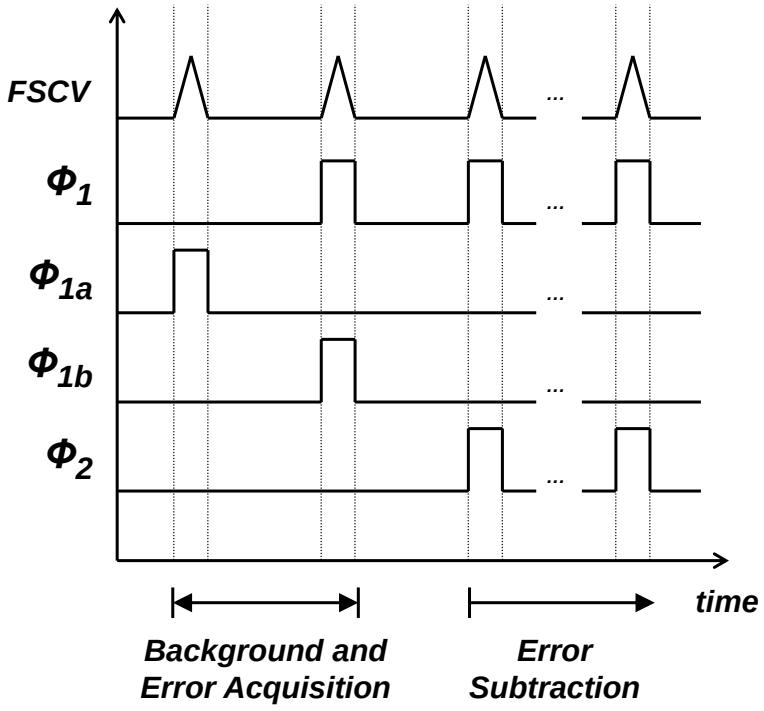

Figure 2.7: Timing diagram of the proposed two-step A/D converter.

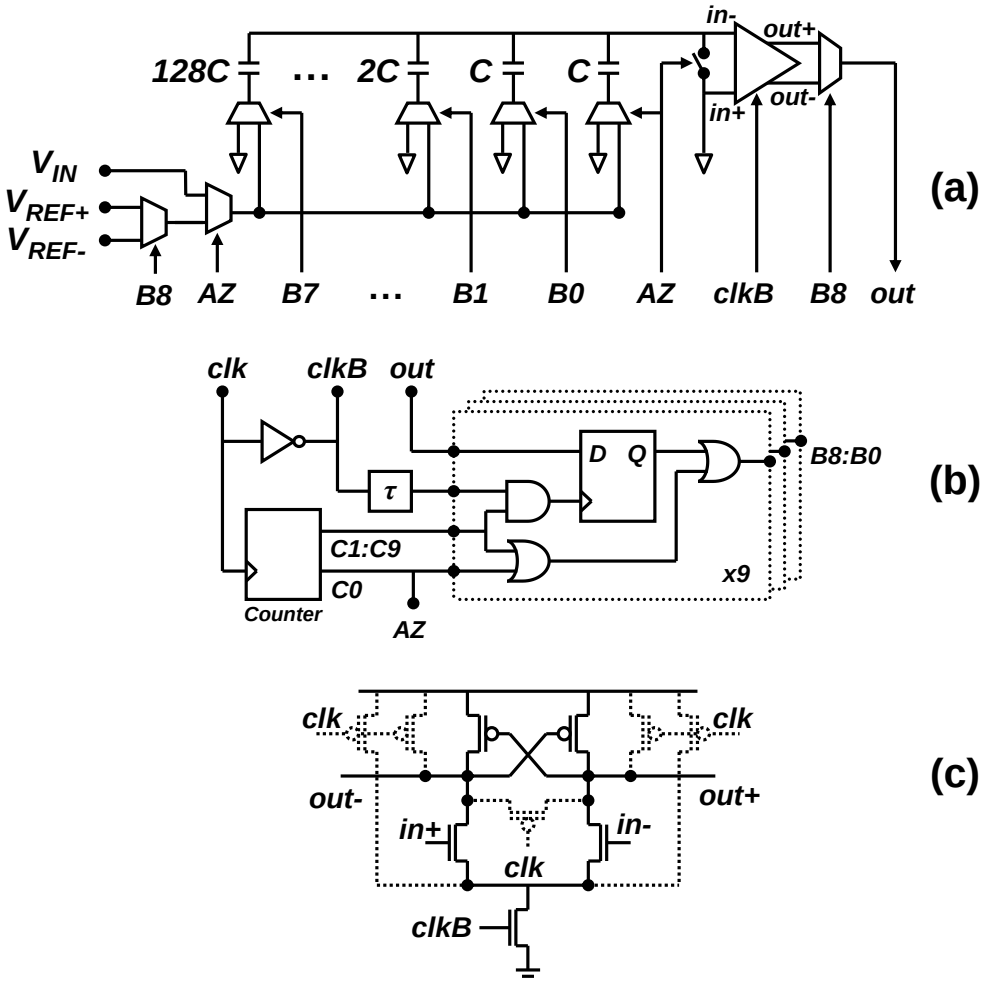

Figure 2.8: (a) 9-bit SAR-ADC with its (b) control logic and (c) comparator.

the second bit cycle, $C1$, the bottom plates are switched to ground, causing the top plates to hold a voltage equal to $-v_{IN}$. This voltage is compared to mid-scale and the outcome of the decision sets the MSB, $B8$, which in turn selects which reference and comparator output will used for the rest of the bit cycles, $C2$–$C9$. When the sampled input is lower than mid-scale (MSB = 0), offset binary encoding is achieved through bitwise negation of the LSBs.

Dynamic Latched Comparator

A latched comparator was chosen due to its low-power nature. To ensure a low offset, the dimensions of both pairs of input and latch transistors were increased well beyond minimum size to mitigate the effects of mismatch and process variations. The comparator operates on both phases of the clock. At the negative edge, its output and tail nodes are precharged to V_{DD} through the dashed-lined PMOS transistors in Figure 2.8(c). At the positive edge, the dynamic latch amplifies the difference across the input in a regenerative manner. The output of the comparator is latched after a short delay greater than the latch's regeneration time of ~20 ns.

2.6.2 Multiplying DAC

The core of the ADC is a switched-capacitor-based multiplying digital-to-analog (D/A) converter (MDAC), which achieves a high linearity by combining input sampling, D/A conversion, analog subtraction, and residue amplification into a single all-in-one block. Figure 2.9 shows a circuit diagram of the 9-bit, switched-capacitor MDAC block with offset cancellation. The MDAC uses an identical

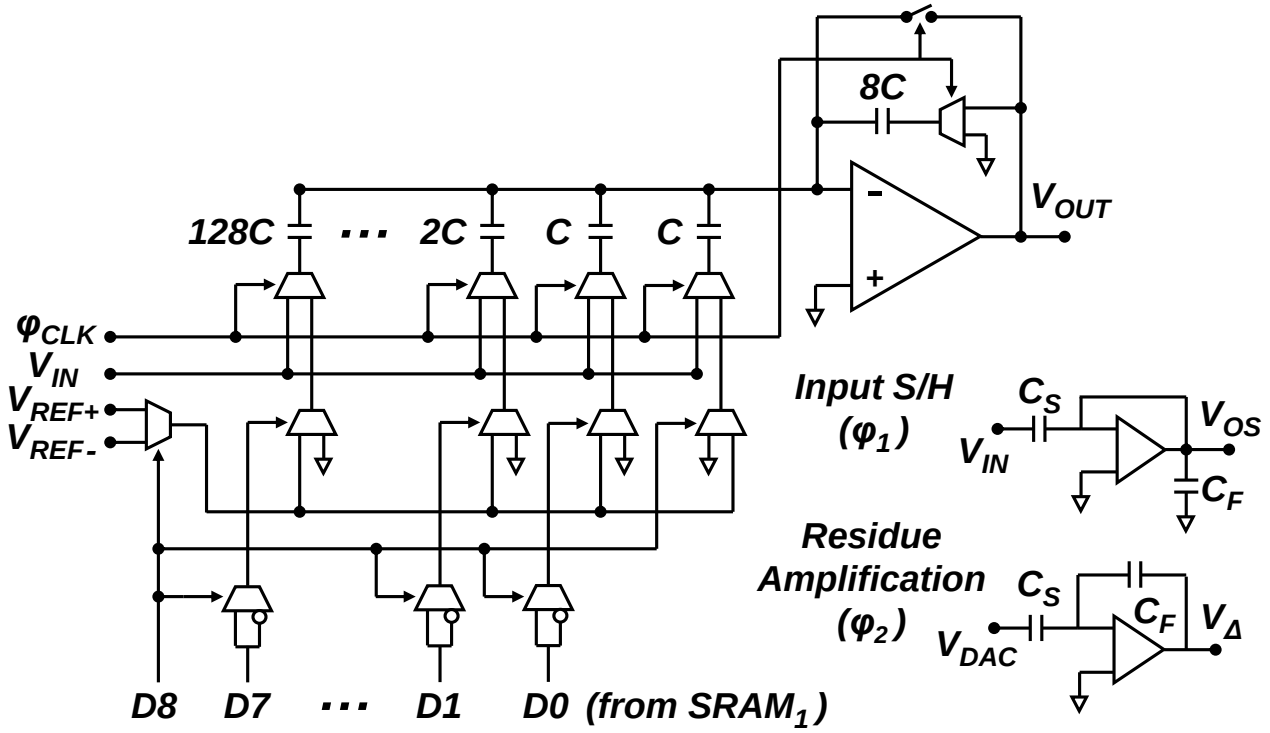

Figure 2.9: Schematic diagram of the switched-capacitor-based multiplying digital-to-analog converter (MDAC) circuit.

copy of the capacitor array in the SAR-ADC. A two-stage folded-cascode operational amplifier (op-amp) with simulated open-loop gain of 77 dB, unity-gain bandwidth of 3 MHz and phase margin of 65° is used as the residue amplifier. The op-amp draws 21 μA from a 1.2-V supply but is duty-cycled to draw an average current of 2 μA.

Reference voltages V_{REF+} and V_{REF-} are set to 1.2 V and 0 V, respectively, to yield a full-scale range that spans the entire supply. The MDAC uses offset binary encoding to avoid bootstrapping and enable low-power operation from a 1.2-V supply. In this encoding scheme, the MSB ($D8$) of the data stored in $SRAM_1$ simultaneously controls which reference gets selected and performs the necessary bit negation of the LSBs ($D7$–$D0$).

2.6.3 Timing

Figure 2.10 shows the timing diagram of the core ADC. A hundred samples are acquired at a sampling rate of 10 kHz during each 10-ms FSCV scan. Each 100-μs conversion consists of a 10-μs input sample-and-hold (S/H) phase (φ_1) and a 90-μs residue-amplification phase (φ_2) to accommodate the op-amp settling times during each of the phases. During the input S/H phase, the capacitor array samples the input while the feedback capacitor samples the offset of the amplifier. During the second phase, the LSBs of the data stored in $SRAM_1$ decide whether each capacitor in the array is connected to the MSB-selected reference or to mid-scale. The ratio between the sampling and feedback capacitances yields a residue amplification closed-loop gain of $A = 32$ in this phase.

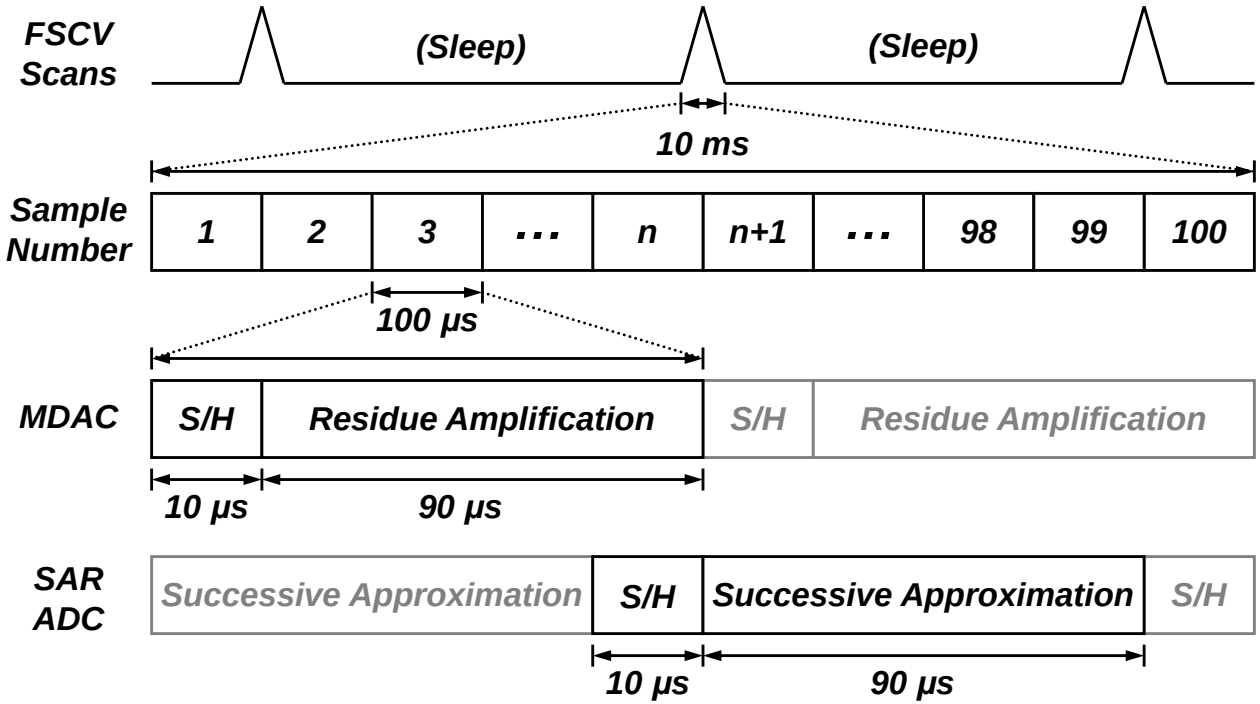

Figure 2.10: Timing diagram of the two-step cyclic ADC.

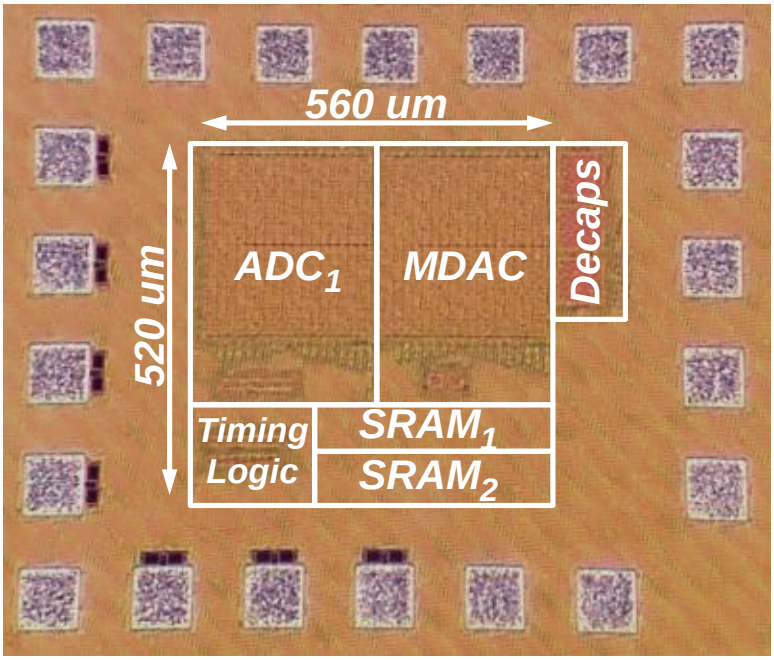

Figure 2.11: Annotated ADC chip micrograph.

2.7 Measured Results

An experimental ADC prototype was fabricated in a 65-nm CMOS process. Figure 2.11 shows a micrograph of the fabricated chip. The prototype occupies an active area of 0.3 mm^2. The op-amp in the MDAC consumes 25 μW of quiescent power off a 1.2-V supply but is shut down during the sleep period between FSCV scans, yielding an effective duty-cycled power consumption of 2.5 μW. The digital blocks and the two capacitor arrays consume a dynamic power of 0.4 μW at a sampling rate of 10 kHz, yielding a total ADC power consumption of less than 3 μW, excluding the digital power from the output drivers.

2.7.1 Device Characterization

A test setup consisting of a 12-bit DAC (Analog Devices AD7392) and a microcontroller (Atmel ATMega644P) was used to test the performance of the ADC at a sampling rate of 10 kHz. A periodic train of 10-ms long, sinusoidal cycles with amplitudes of 300 mV and 310 mV were reproduced via direct digital synthesis every 100 ms to imitate the typical background and dopamine-induced excursions observed in 300-V/s FSCV at the output of the sensing interface. Real-time output background-subtracted data was collected directly from the ADC. Figure 2.12 illustrates the measured background-subtracted output voltage versus the expected 10-mV sine difference after the background acquisition and subtraction step, ϕ_1, described in Section 2.3.1 (Fig. 2.12(a)), after the error subtraction step, ϕ_2, described in Section 2.3.2 (Fig. 2.12(b)), and after a subsequent offline 9-point smooth (Fig. 2.12(c)). Each step reduces further the ADC quantization error.

It is important to understand that the proposed two-step ADC does not digitize absolute input voltages but rather resolves directly small input voltage differences relative to an arbitrary baseline. Thus, to test the ADC static linearity, the input voltage was swept linearly in the range of ±10 mV in steps of 50 μV relative to an arbitrary DC offset using a *Keithley* 2400 source-measure unit. Figure 2.13 shows the measured output voltage for baseline-subtracted differential input voltages ranging from −10 mV to +10 mV. The non-linearity of the op-amp in the MDAC block limits the overall static linearity of the ADC.

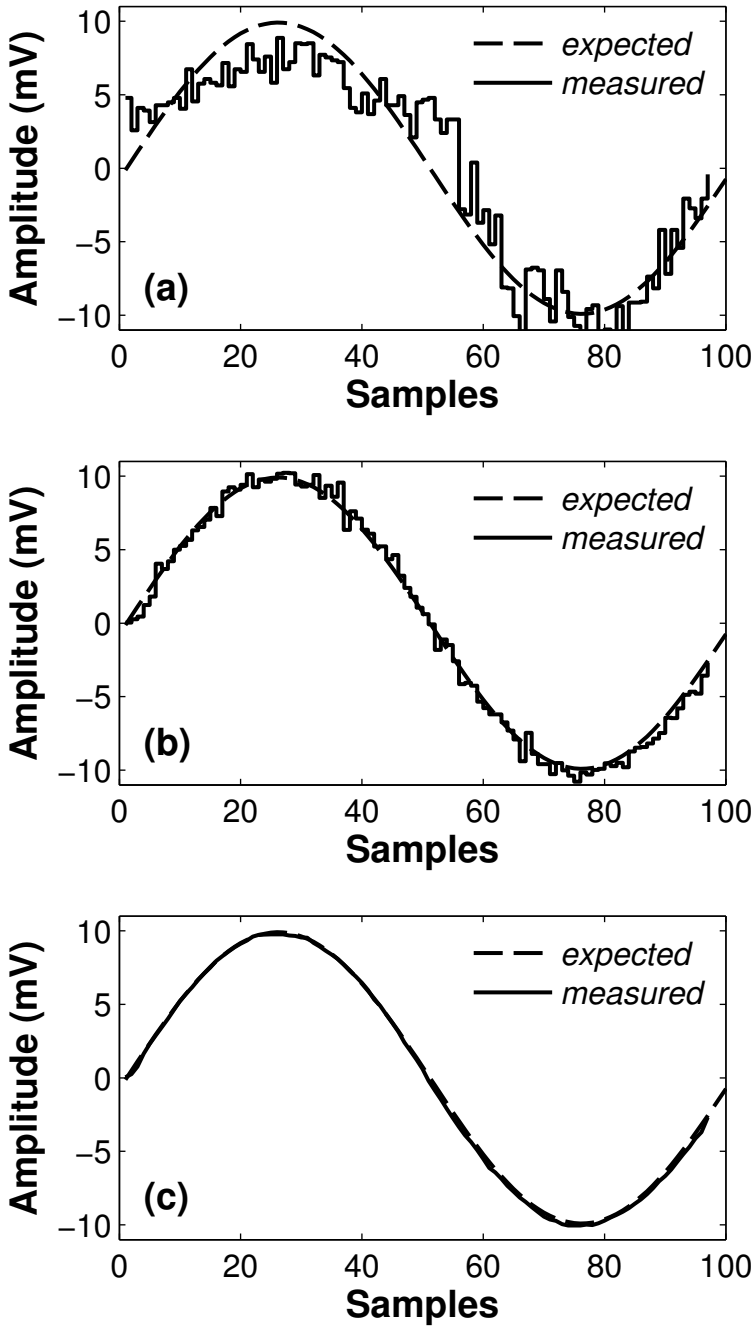

Figure 2.12: Measured output for one cycle of a 10-mV differential input sinusoid: (a) after the background acquisition and subtraction step, ϕ_{1b}, described in Section 2.3.1, (b) after the error subtraction step, ϕ_2, described in Section 2.3.2, and (c) after an offline 9-point smooth.

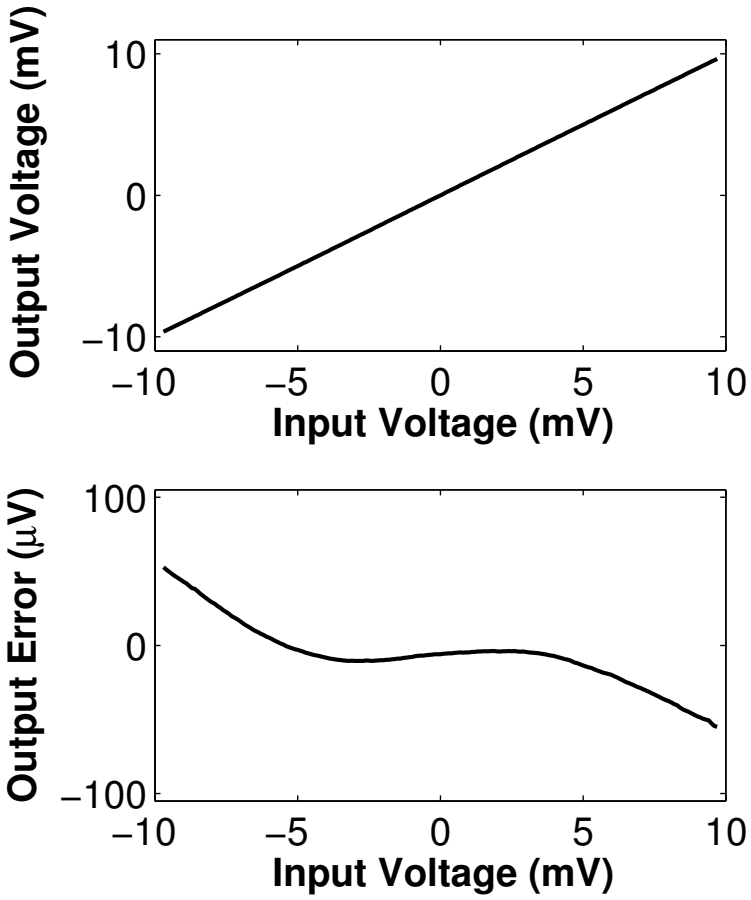

Figure 2.13: Measured static linearity of the A/D converter for differential input voltages in the range of −10 mV to +10 mV.

2.7.2 Device Validation

For proof-of-concept detection of dopamine *in vitro*, a carbon-fiber microelectrode (CFM) consisting of a single carbon fiber inside a 1.8 mm glass capillary tube was fabricated, as described in [27]. The glass capillary tube was heated in the middle and pulled to form a tight seal around the carbon fiber at one end. The carbon fiber was cut at this end so that a segment of approximately 100 μm protruded from the glass seal. A chlorinated silver wire soldered onto a gold pin was inserted into the glass capillary tube at the opposite end. To promote electrical conduction between the carbon fiber and the chlorinated silver wire, a 3M KCl solution was injected into the glass capillary tube. A reference electrode consisting of another chlorinated silver wire was also soldered onto a gold pin. A simple in-house flow system was used to validate the chip. The CFM and reference electrode were immersed into a small petri dish filled with a buffer solution representing physiological ion concentrations. The buffer solution contained: 140 mM NaCl, 5 mM KCl, 5 mM $CaCl_2$, 1 mM $MgCl_2$, and 10 mM HEPES. NaOH was added to elevate the pH to 7.3. On the same day of the experiment, a dopamine hydrochloride powder was diluted in buffer solution to achieve a concentration level of 2 μM.

The ADC was interfaced to a signal conditioning frontend comprised of a transimpedance amplifier (Texas Instruments OPA364) with a gain of 1 V/μA and a unity-gain difference amplifier (Texas Instruments INA132). The output reference terminal of the difference amplifier was connected to a 0.5-V reference voltage to offset the output signal. The working and reference electrodes were connected to the frontend. Prior to recording, consecutive 300-V/s, 10-Hz FSCV scans were applied to the CFM for least 20 minutes to stabilize the electrode. In

each scan, the applied voltage was swept from a resting value of −0.4 V to a peak value of +1.0 V and back to its resting value. One (1) minute after the start of the recording session, a syringe was used to introduce a bolus of dopamine to replace the buffer solution. Two (2) minutes after dopamine injection, buffer solution was introduced to replace the dopamine solution. The CFM was kept immersed in the buffer solution during the entire recording session. Real-time FSCV measurements were collected for a duration of 5 minutes. The measured background and background-subtracted currents were plotted against the applied voltage to yield background and background-subtracted cyclic voltammograms, respectively.

Figure 2.14 shows the FSCV measurements collected at the CFM during the *in vitro* recording session. Figure 2.14(a) shows a background voltammogram (average of 10 scans) obtained in buffer solution alone at the end of the recording. Figure 2.14(b) shows a background-subtracted voltammogram (average of 10 scans) obtained directly from the ADC at just before dopamine washout at t = 3 minutes. The peak currents near +0.55 V and −0.25 V vs. Ag/AgCl correspond to dopamine oxidation and reduction, respectively. Figure 2.14(c) shows the time course of the measured dopamine oxidation current at +0.55 V (arrow in Figure 2.14(b)) throughout the 5-min recording session. The time course of the current reflects the dopamine concentration at the CFM. As seen in Figure 2.14(c), dopamine increases after injection at t = 1 minute and decreases after washout at t = 3 minutes. An ADC sensitivity of ~150 pA_{rms} was obtained from the trace in Figure 2.14(c). Figure 2.15 illustrates a three-dimensional pseudocolor plot of all consecutive background-subtracted voltammograms collected during the recording. Each pixel column in Figure 2.15 represents an individual background-subtracted voltammogram acquired during a single FSCV scan,

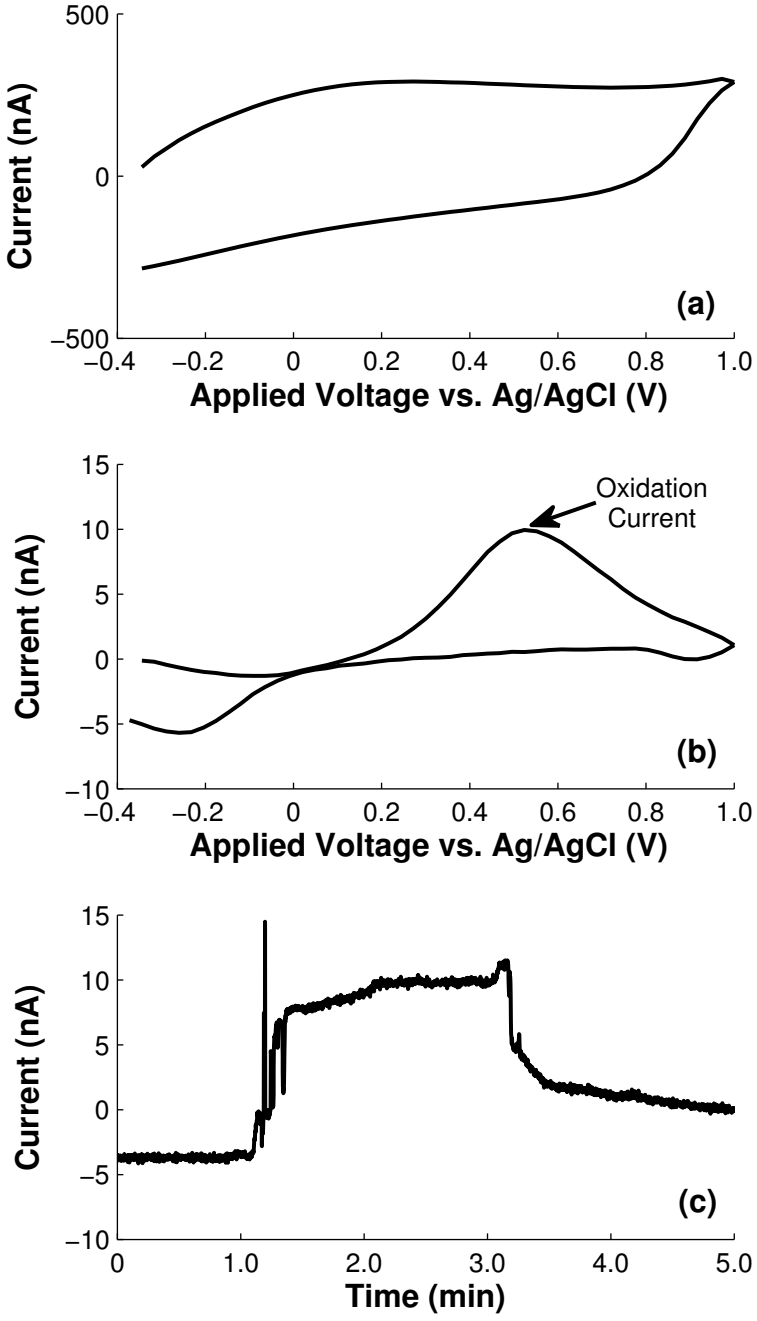

Figure 2.14: FSCV *in vitro* measurements recorded at a CFM during flow-injection of 2-μM dopamine (DA). (a) Background voltammogram (average of 10 scans) in buffer alone. (b) Background-subtracted voltammogram (average of 10 scans) during DA injection. (c) Time course of peak DA oxidation current. DA injection and DA washout occurs at t = 1 min and t = 3 min, respectively.

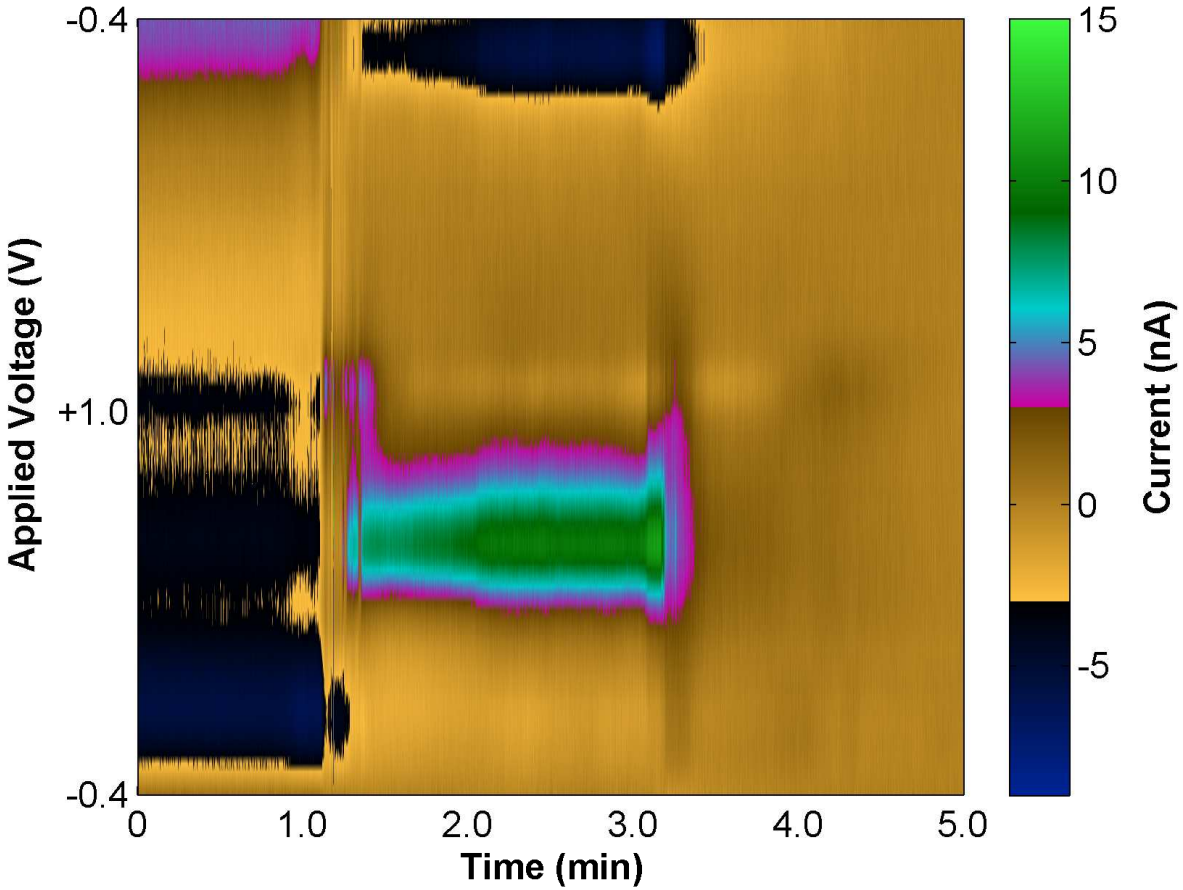

Figure 2.15: 3-D pseudo-color plot of consecutive background-subtracted voltammograms collected at a CFM during flow-injection of 2-μM dopamine. The x-axis shows the time course, the y-axis denotes applied voltage, and the z-axis (color axis) depicts the magnitude of the current.

starting at the bottom of the column and ending at the top. Similarly, each pixel row represents the time course, in 100-ms steps, of the background-subtracted current at a fixed applied voltage. The color gradient depicts the magnitude of the current.

2.8 Non-idealities

It should be noted that offset errors due to component mismatch only contribute second-order degradation effects to the overall dynamic range of the system. To include the effect of these non-idealities in the analysis presented in Section 2.3, an offset error term is added to each of the residues v_Δ, $v_{\Delta 1}$, and $v_{\Delta 2}$ in Equation 2.4 and Equation 2.5, yielding

$$v_\Delta \rightarrow v_\Delta + v', \tag{2.13a}$$

$$v_{\Delta 1} \rightarrow v_{\Delta 1} + v'_1, \tag{2.13b}$$

$$v_{\Delta 2} \rightarrow v_{\Delta 2} + v'_2, \tag{2.13c}$$

where v', v'_1, and v'_2 are the offsets from conversion of the background, amplified residue, and amplified output, respectively. Binary subtraction of Equation 2.4 from Equation 2.5 with the new values in Equations 2.13a–2.13c yields

$$v_{out_2} = v_{out} - \frac{v_{\Delta_2} - v_{\Delta_1}}{A} - \frac{(v'_2 - v'_1)}{A}. \tag{2.14}$$

Comparing Equation 2.6 and Equation 2.14, it is evident that the latter introduces negligible degradation due to full cancellation of v' and partial attenuation of v'_1 and v'_2 by the gain A of the amplifier.

2.9 Summary

In this chapter, we presented a dynamic range enhancement technique for integrated wireless neurochemical monitoring systems and introduced a novel two-step cyclic ADC architecture that implements the proposed scheme with very low power consumption. With an effective resolution of ~14 bits, the proposed system should theoretically be able to resolve *faradaic* currents as small as 61pA in background currents of ±500nA, a performance comparable to that of a recent state-of-the-art design [43]. We also demonstrated functionality of the system through real-time detection of 2-μM dopamine using FSCV. Preliminary measured results indicated the system was capable of detecting directly *faradaic* currents in the range of ±10 nA with a sensitivity of ~150 pA.

In the next chapter, we will show how the proposed scheme relaxes the data rate requirement of the wireless link by discarding redundant background information before wireless transmission. We will also demonstrate on-chip integration of the ADC architecture described in this chapter with low-power sensing frontend and impulse-radio transmitter blocks for ultra-low-power telemetry using FSCV *in vitro*.

CHAPTER 3

A WIRELESS IC WITH ANALOG BACKGROUND SUBTRACTION AND UWB TELEMETRY FOR NEUROCHEMICAL MONITORING USING FAST-SCAN CYCLIC VOLTAMMETRY

3.1 Introduction

Dopamine is a neurotransmitter that plays a fundamental role in motor control [23] and reward-seeking behaviors including drug addiction and eating disorders [4]. Fast-scan cyclic voltammetry (FSCV) has become the most widely used electrochemical method for studying the intricate relationship between brain dopamine release and behavior [19]. With its subsecond temporal resolution and high chemical selectivity, it is the preferred technique for monitoring rapid changes in dopamine concentration levels in ambulatory subjects during brain-behavior studies [40].

Recent technological advances have enabled miniaturized devices that can achieve stress-free, wireless FSCV monitoring of dopamine release in freely-moving small animals [35, 41]. The main drawback of these battery-operated systems is their limited power budget. Resolving wide-range neurochemical signals with high chemical and temporal resolution mandates high-precision conversions and high sampling rates, and thus, high wireless transmission data rates, which considerably decrease battery life. Long-term monitoring in complex, enriched environments is a promising research direction in behavioral neuroscience that can provide further insights into behaviors such as social interaction and reward-based learning [12, 20]. To enable these long-term behavioral studies, wireless FSCV systems must implement energy-efficient data ac-

quisition and wireless transmission schemes that meet the stringent dynamic range requirements of FSCV with minimal power.

In FSCV, the electrode potential is scanned periodically with a triangular waveform, and the resulting current is measured. A drawback of the technique is the large background current produced due to charging of the double-layer capacitance of the electrode-electrolyte interface [40]. This background current can be several hundred times larger than the small redox current indicating dopamine concentration. Recent wireless FSCV microsystems have overcome this limitation by implementing high-order delta-sigma ($\Delta\Sigma$) modulation techniques to acquire the entire span of the background with reduced in-band quantization noise at the expense of increased wireless data transmission rates [7,42,43]. Since the background is remarkably stable over short times [25], these systems waste a significant fraction of their limited power budget repeatedly resolving and transmitting the same background information over consecutive scans. In theory, these systems can achieve the same dynamic range at lower data rates by systematically removing the redundant background before transmission.

This chapter presents a low-power wireless FSCV monitoring IC that directly extracts and transmits only the relevant background-subtracted redox current; i.e. the dopamine signal. The chip achieves a dynamic range comparable to that of state-of-the-art wireless FSCV microsystems albeit at a fraction of the power. Two key insights enable the improved performance. First, we make use of the analog-to-digital converter (ADC) architecture described in Chapter 2, which leverages the fact that the background is a periodic signal with a known quantization error to increase the dynamic range without noise shaping. The two-step

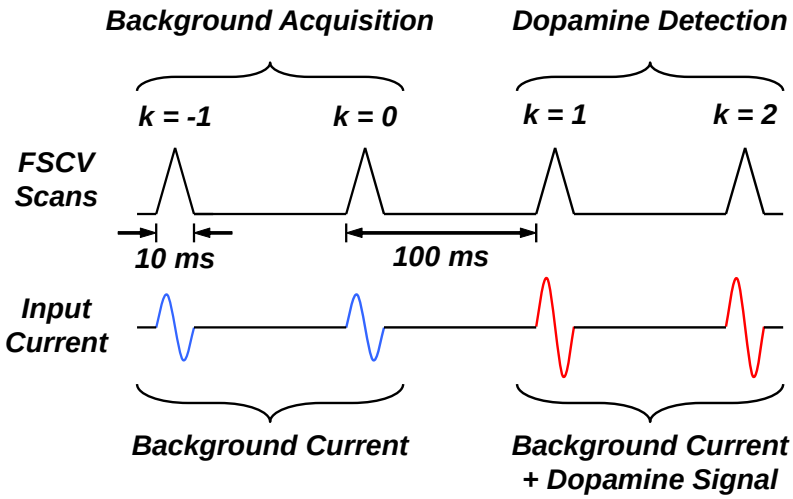

Figure 3.1: Electrochemical detection of dopamine using fast-scan cyclic voltammetry (FSCV) at a carbon-fiber microelectrode (CFM). For simplicity, a sinusoidal model with time-varying amplitude is used for the input current collected from the CFM.

cyclic ADC achieves an extended dynamic range by performing real-time analog and digital background subtraction on-chip. By removing the background before transmission, the data rate requirement of the transmitter (TX) is also reduced. Second, we make use of a duty-cycled impulse-radio ultra-wideband (IR-UWB) TX, with power directly proportional to the data rate, which takes advantage of the reduced data rate to achieve wireless transmission with minimal power consumption.

3.2 Analog Background Subtraction

In 300-V/s FSCV at a CFM, a sequence of 10-ms triangle waveforms is applied to the electrode every $T = 100$ ms, as shown in Figure 3.1. In the absence of dopamine, the total input current is equal to the background current. In the

presence of dopamine, the total input current is the sum of the background current and a time-dependent dopamine signal. Because the background is stable immediately before and after dopamine release, it can be modeled as a periodic signal $\tilde{x}_{bg}$ with period T, for which

$$\tilde{x}_{bg}(t + kT) = x_{bg}(t), \quad k \in \mathbb{Z}. \tag{3.1}$$

Using Equation 3.1 and assuming dopamine release occurs at $k > 0$, the input current x_k collected on the k^{th} scan is given by

$$x_k = \begin{cases} \tilde{x}_{bg} + x_{da,k} & , \quad k > 0 \\ \tilde{x}_{bg} & , \quad k \leq 0 \end{cases} \tag{3.2}$$

where $x_{da,k}$ is the time-dependent dopamine signal on the k^{th} scan. Conversion of x_k using an N-bit ADC yields a quantized signal $\hat{x}_k$ with a quantization error ϵ_k given by

$$Q\{x_k\} = \hat{x}_k = x_k + \epsilon_k. \tag{3.3}$$

where Q is the quantization operator, and ϵ_k has a quantization width $\Delta = R/2^N$, where R is the ADC's full-scale range. Typically, numerical background subtraction in software is used to recover the dopamine signal. In this case, a copy of the background current acquired just before dopamine release ($k = 0$) is subtracted from the total current acquired during dopamine detection ($k > 0$). Thus, for $k > 0$, the output y_k after numerical background subtraction can be written as

$$y_k = \hat{x}_k - \hat{x}_0. \tag{3.4}$$

Applying Equation 3.2 and Equation 3.3 to Equation 3.4 yields

$$y_k = x_{da,k} + \epsilon'_k, \tag{3.5}$$

where $\epsilon'_k = \epsilon_k - \epsilon_0$ has a quantization width Δ' given by

$$\Delta' = x_{\max}/2^{N-1}, \tag{3.6}$$

where x_{max} is the maximum amplitude of the input current x_k, which also spans the full-scale range of the ADC. Equation 3.6 implies that accurate measurement of the very small dopamine signal requires a high-resolution N-bit ADC, where N is large. This is true even though many of the most significant bits are wasted on resolving the ever-present background signal that contains no new information. The need for a high-resolution ADC drives up the power budget for such systems.

Several techniques such as analog offset compensation [28], analog filtering [8], and analog background subtraction [27], have been proposed to reduce the size of the background current before conversion and thus increase the dynamic range of the ADC. Because the actual background is a complex and nonlinear waveform, linear techniques such as offset compensation and filtering only achieve partial removal of the background. To circumvent this limitation, we present an analog background subtraction technique, as illustrated in Figure 3.2 and Figure 3.3, that performs coarse and fine quantization of the dopamine-free background signal over two consecutive FSCV scans. During the first scan ($k = -1$), a coarse copy of the background signal is digitized and stored in memory $SRAM_1$ (solid blue line in Figure 3.2a). During the second scan ($k = 0$), this coarse background copy is subtracted from a second background signal (dashed blue line in Figure 3.2a) in the analog domain to recover the periodic quan-

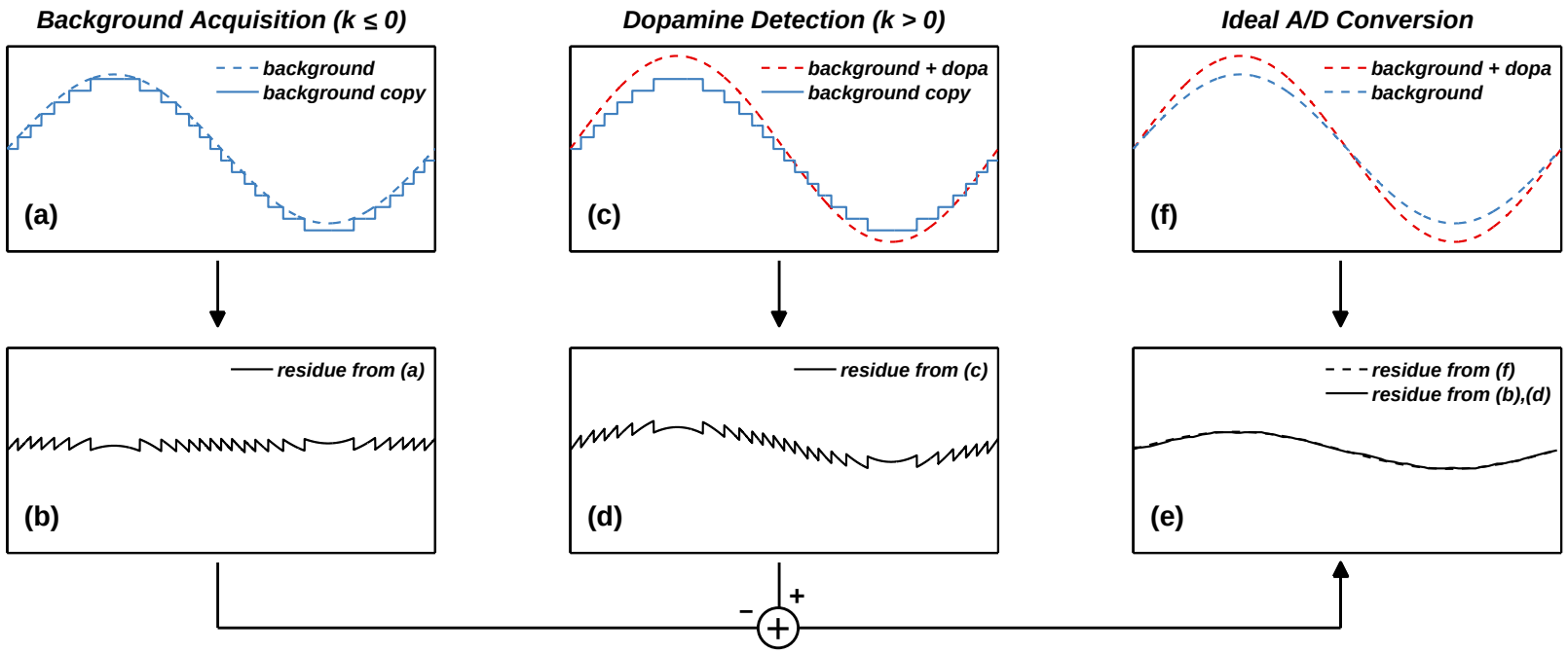

Figure 3.2: Illustration of N-bit A/D conversion with analog background subtraction (a)-(e), versus ideal $N + M$-bit A/D conversion (f).

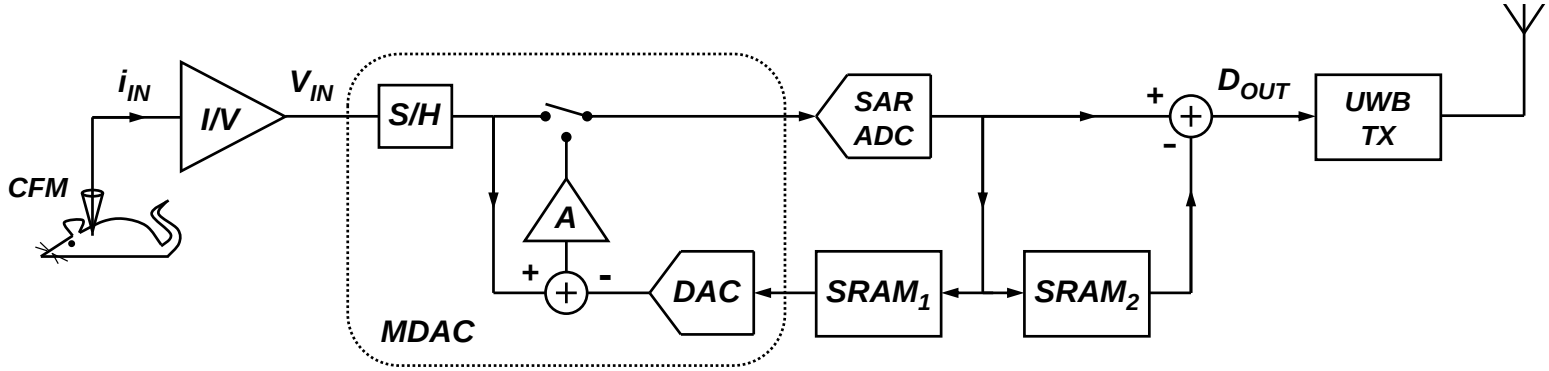

Figure 3.3: Simplified block diagram of the wireless FSCV monitoring microsystem with on-chip analog background subtraction and UWB telemetry.

tization error of the background (Figure 3.2b), which is quantized and stored in memory $SRAM_2$. The sum of these two stored signals (*coarse* background + *fine* quantization error) is used to reconstruct a high-resolution background copy using a low-resolution ADC. This high-resolution copy is subsequently subtracted from the input signal during dopamine detection ($k > 0$) to recover the dopamine signal (Figure 3.2c–3.2e). Thus, for $k > 0$, the output y_k after analog background subtraction can be written as

$$y_k = \frac{Q\{A(x_k - \hat{x}_{-1})\} - Q\{A(x_0 - \hat{x}_{-1})\}}{A}, \tag{3.7}$$

where A is the gain of the rail-to-rail amplifier block in Figure 3.3 needed to scale the background-subtracted residues (Figs. 3.2b and 3.2d) to span the ADC full-scale range. Choosing $A = 2^M$, and applying Equation 3.2 and Equation 3.3 to Equation 3.7 yields

$$y_k = x_{da,k} + \epsilon_k'', \tag{3.8}$$

where $\epsilon_k'' = (\epsilon_k - \epsilon_0)/2^M$ has a width Δ'' given by

$$\Delta'' = x_{\max}/2^{(N+M)-1}. \tag{3.9}$$

Comparing Equation 3.6 and Equation 3.9 reveals analog background subtraction provides M additional bits of resolution for the same N-bit conversion. This increase in resolution compares favorably to that achieved through $\Delta\Sigma$ modulation, which roughly provides $L + 0.5$ additional bits of resolution, where L is the modulator's order, for each doubling of the oversampling ratio OSR. To achieve a dynamic range of $N + M$ bits, where $N + M$ is large, a single-bit $\Delta\Sigma$ modulator

requires an OSR given by

$$OSR = \left(2^{N+M}\frac{\pi^L}{\sqrt{2L+1}}\right)^{\frac{1}{L+0.5}}. \tag{3.10}$$

Plugging $N = 9$ and $M = 5$ for the values used in this work and $L = 3$ for the third-order modulator in [42] into Equation 3.10 yields an OSR of 32. This result indicates that even with the use of a high-order modulator, which increases design complexity and power consumption, a third-order ΔΣ ADC still requires 32× the sampling rate of the Nyquist ADC used in this work given the same dynamic range requirement. The reduced sampling rate in our work relaxes the wireless data rate requirement as follows. In a Nyquist ADC, the serialized unencoded data rate R_b is given by

$$R_b = N \times f_s, \tag{3.11}$$

where N is number of bits per sample, and f_s is the Nyquist sampling rate. In an oversampling ΔΣ ADC, the undecimated unencoded data rate R_b' is given by

$$R_b' = OSR \times f_s. \tag{3.12}$$

In [7, 42, 43], the unencoded data rate of the transmitter is equal to the undecimated data rate of the ΔΣ modulator because the decimation filter is implemented on the receiver side due to its complexity, area and power. Comparing Equation 3.11 and Equation 3.12 with $N = 9$ and $OSR = 32$ reveals the ADC in this work yields a 3.5× reduction in the wireless data transmission rate compared to the ADC in [42]. Assuming a wireless link with power directly proportional to the data rate, such as in a duty-cycled IR-UWB TX, this reduction

also yields a 3.5× decrease in transmit power, the main component of the power budget in low-power wireless sensing systems.

3.3 UWB Telemetry

There has been considerable interest in UWB telemetry for high-data-rate biomedical applications requiring short-range, low-power wireless transmission. The inherent wide-spectrum of UWB signals (>500 MHz) provides the bandwidth needed for multi-channel simultaneous recording [9, 29]. UWB telemetry also offers numerous advantages for low-data-rate, energy-starved monitoring applications. The short duration of UWB pulses (~2 ns) allows aggressive duty-cycling of the wireless link between consecutive pulses to achieve substantial power savings. In [14], we demonstrated duty-cycled IR-UWB radios consume considerably less power compared to narrowband systems at low data rates. This is because average power P_{avg} in a duty-cycled IR-UWB TX is linearly proportional to the data rate R_b, as given approximately by

$$P_{avg} = E_b \cdot R_b + P_0, \tag{3.13}$$

where E_b is the energy efficiency (or energy per pulse), and P_0 is a constant representing leakage and overhead power. Equation 3.13 suggests that for energy efficiencies in the order of 100 pJ/pulse, duty-cycled IR-UWB transmitters operating at a data rate of 100 kbps consume a few tens of microwatts, compared to the milliwatt power consumption of the narrowband systems in [7, 42, 43]. This orders-of-magnitude reduction in TX power associated with duty-cycled IR-UWB telemetry is critical to enable long-term brain-behavior studies.

3.4 System Architecture

As noted in Section 3.1, the key insight of this work is the combination of a transmitter topology for which the power consumption depends linearly upon the transmit data rate, and a data minimizing ADC that eliminates redundant background signals by design. Together, these two elements yield the low-power wireless FSCV microsystem depicted in Figure 3.3, which operates as follows. A sequence of 300-V/s, 10-Hz FSCV scans generated off-chip is applied to a CFM via a low-noise potentiostat that also performs current-to-voltage (I/V) conversion. A 9-bit two-step cyclic Nyquist ADC performs analog background subtraction, as described in Section 3.2, to directly resolve the dopamine signal during each 10-ms scan at 10-kS/s conversion rate. As described in Section 3.2, memories $SRAM_1$ and $SRAM_2$ are used to store the *coarse* and *fine* background copies during background acquisition. Both of the stored signals are subtracted from the input signal during dopamine detection to yield the background-subtracted dopamine signal. A stop bit is added to each 9-bit sampled data to form a 10-bit word that is then serialized at a data rate of 100 kbps. The serialized bit-stream is encoded at the IR-UWB TX into FCC-compliant pulses that are wirelessly transmitted via an off-chip surface mount UWB antenna to an external IR-UWB receiver (RX), previously demonstrated in [48], which achieves robust synchronization through a novel pulse-coupled oscillator scheme developed in [47].

3.5 Circuit Implementation

3.5.1 Low-Noise Potentiostat

Figure 3.4 shows the schematic diagram of the low-noise potentiostat used in this work. The circuit is based on the current-mirror-based potentiostat described in [1] for a two-electrode electrochemical sensor. A two-electrode system is used in this work because the small currents involved in 300-V/s FSCV at a CFM produce a negligible ohmic drop that does not affect the reference electrode (RE) [36]. The potentiostat is a regulated common-gate (RCG) stage, also known as a regulated cascode amplifier (RCA) [3], consisting of a high-gain differential amplifier $A(s)$ and transistor M_1. The negative feedback loop in the RCG stage serves a three-fold purpose. First, it ensures that the potential of the working electrode (WE) is identical to the potential V_{SCAN}. Second, it reduces the input resistance of M_1 by the gain of the amplifier, ensuring that all of the input current i_{IN} collected from the sensor is buffered to the drain of M_1. Third, it increases the output resistance of M_1 by the amplifier's gain, ensuring that all of the buffered current is mirrored by an active current mirror onto resistor R_P to produce a voltage V_{IN} that is fed to the input of the ADC.

A transimpedance gain R_P of 1 MΩ is used, followed by a unity-gain output buffer, which decreases the output resistance of the potentiostat. A single-stage, folded-cascode amplifier with a simulated open-loop gain of 50 dB and 3-dB bandwidth of 10 kHz is used for both the RCG feedback amplifier and the output buffer in the potentiostat. The RCG feedback amplifier draws 2 μA from a 3-V supply. The output buffer draws 10 μA during each 10-ms FSCV scan and is turned off for the 90-ms resting period between scans to save power. Thus, the

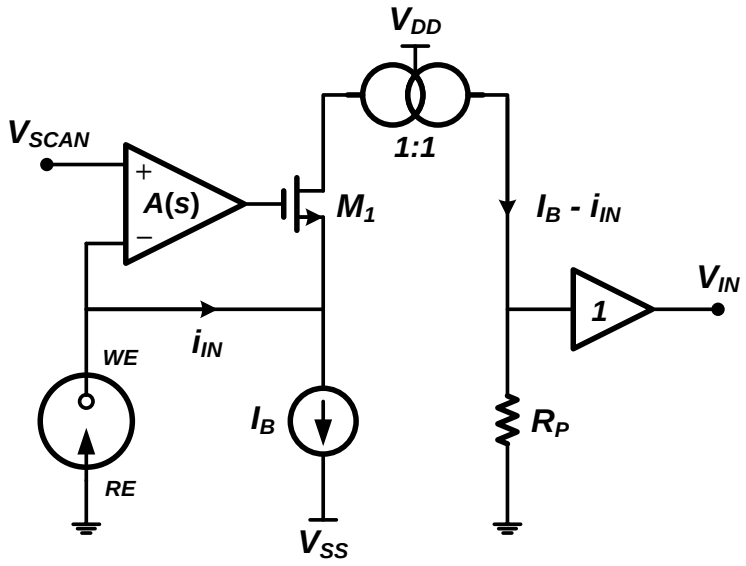

Figure 3.4: Schematic diagram of the current-mirror-based potentiostat, based on [1], designed for a two-electrode electrochemical cell.

duty-cycled buffer draws 1 μA from a 3-V supply. A bias current I_B is also used to allow the measurement of bidirectional redox currents [21].

3.5.2 Two-Step Cyclic ADC

A key design element of this architecture is the two-step cyclic A/D converter previously demonstrated in Chapter 2. The core ADC consists of a successive-approximation (SAR) ADC, a multiplying digital-to-analog converter (MDAC), and two SRAM modules. As shown in Figure 3.3, the core ADC samples the background signal and stores a copy in $SRAM_1$. This quantized signal is then reproduced via a DAC and subtracted from a subsequent scan to form a residue. This signal is amplified to generate a periodic quantization error signal which is stored in $SRAM_2$. Together, these two signals form a high-fidelity background copy.

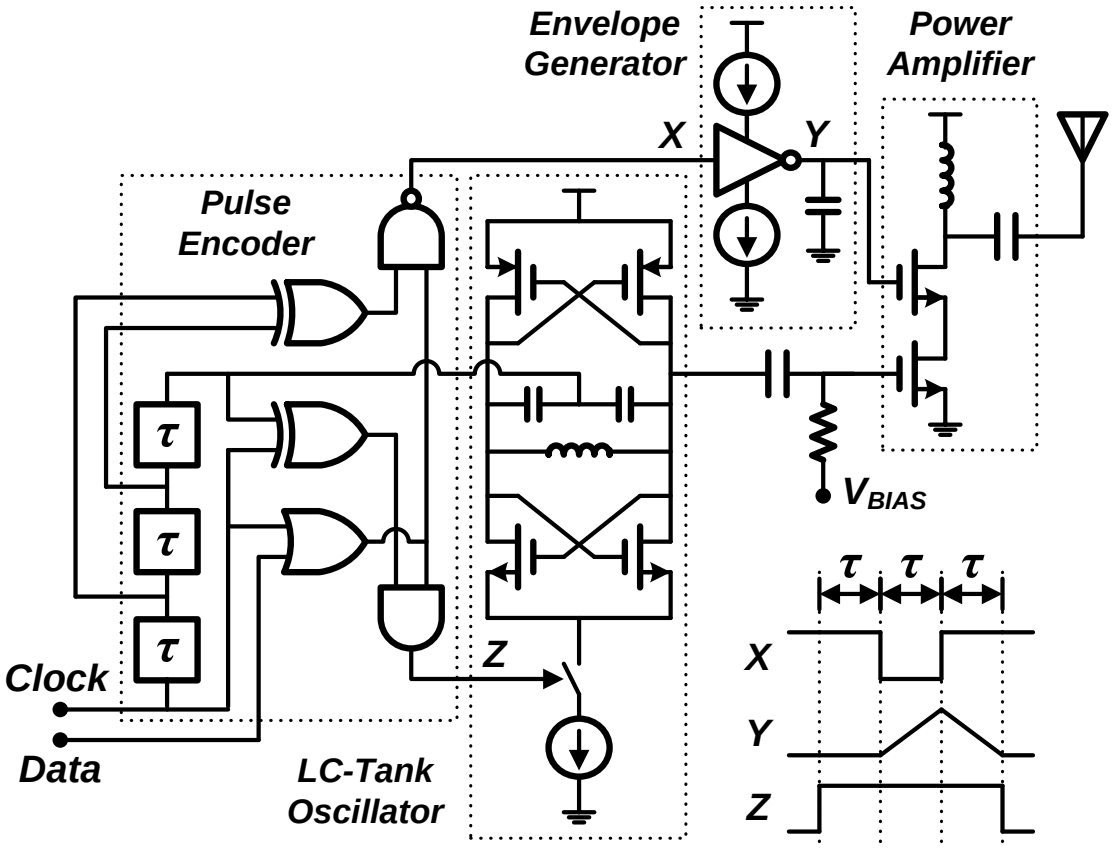

Figure 3.5: Schematic diagram of the duty-cycled UWB transmitter with triangular pulse shaping.

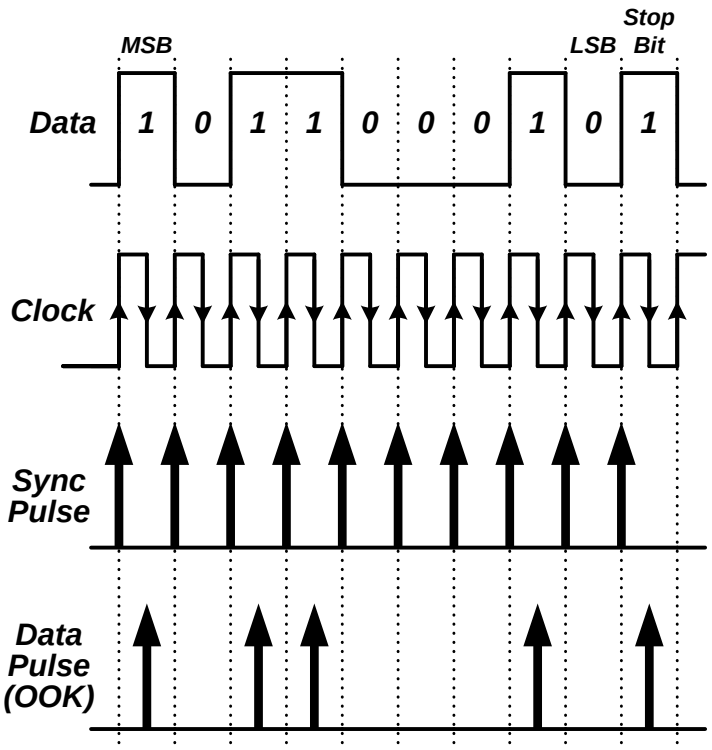

Figure 3.6: Timing diagram of the duty-cycled UWB transmitter with a dual-band *on-off* keying (OOK) pulse encoding scheme.

3.5.3 IR-UWB Transmitter

The other critical design element to enable low power operation is the UWB transmitter. Figure 3.5 shows a schematic diagram of the duty-cycled IR-UWB TX implemented in this work. The topology is a modified version of the architecture in [13] with a unique digital tuning scheme. The TX block is comprised of an *LC*-tank voltage-controlled oscillator (VCO) and a class-C power amplifier (PA). An *LC*-tank oscillator is used over a ring oscillator for superior frequency stability and spectral purity. The design uses two 500-MHz sub-bands in the unlicensed 3.1–10.6 GHz UWB spectrum to transmit two types of pulses: synchronization (*sync*) pulses required for receiver synchronization, and *data* pulses,

which are sent on separate 3.5 and 4.5 GHz channels, respectively, to improve interband isolation on the receiver side. On each rising and falling edge of the clock, a pulse generator outputs an enable signal that turns on the *LC*-tank oscillator for a brief duration to produce short wavelet pulses. As illustrated in Figure 3.6, *sync* pulses are sent on every positive edge of the clock, while *data* pulses are transmitted on the negative edge of the clock using an on-off-keying (OOK) encoding scheme. Triangular pulse-shaping is implemented with a simple charge-pump-based envelope generator to improve the spectral efficiency and to reduce the cross-talk between the two bands.

3.6 Measurement Results

Figure 3.7 shows a micrograph of the IC, which was fabricated in TSMC 65-nm CMOS process. The chip occupies 1.5 mm × 1.0 mm, including the bondpads. The measured average power consumption is 30 μW. The sensing interface, i.e. potentiostat and ADC, consumes 14.4 μW while the IR-UWB transmitter consumes 15.6 μW. The chip was packaged and assembled on a miniature PCB substrate with a few external components for ultra-low-power supply, bias, clock and triangle waveform generation. Figure 3.8 illustrates the miniaturized wireless device, which draws a total average current of only 48 μA from a 3-V coin-cell battery. The device measures 4.7 cm × 1.9 cm and weighs 4.3 g (including the battery and antenna), and thus can be carried by small animals. Table 3.1 summarizes the measured performance of the main circuit blocks of the fabricated chip. Table 3.2 compares the performance of the chip against that of recently published wireless FSCV monitoring microsystems.

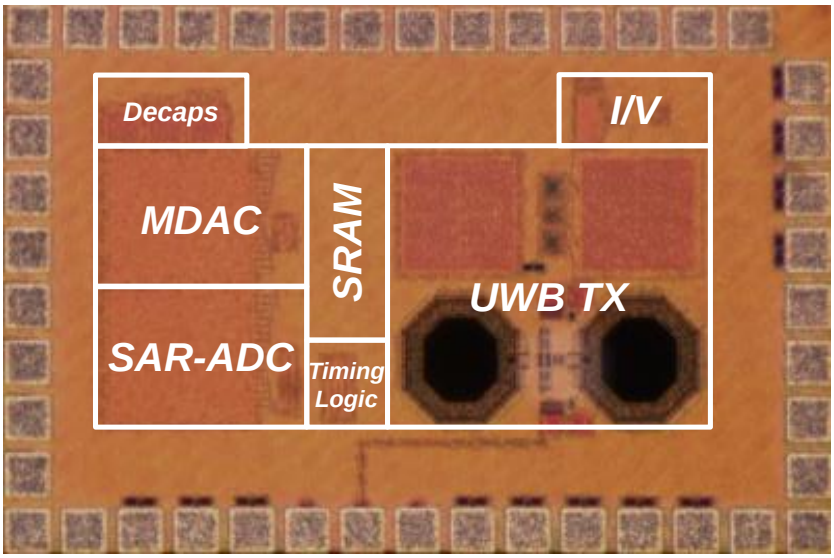

Figure 3.7: Micrograph of the 1.5 mm^2 wireless FSCV monitoring IC.

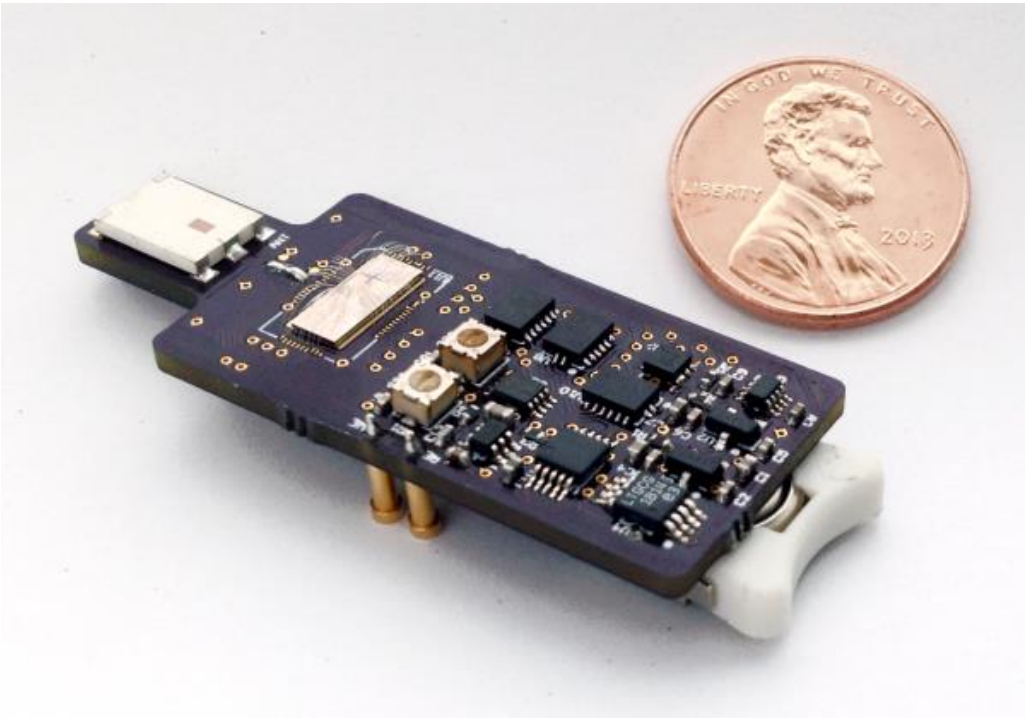

Figure 3.8: Miniaturized wireless device, which operates from a 3-V coin-cell battery, measures 4.7 cm × 1.9 cm, and weighs 4.3 g (with battery and antenna).

Table 3.1: Summary of Measured Performance

Conversion Rate	10 kS/s
Input Current Range	±430 nA
Input-Referred RMS Noise	92 pA
Total Power Consumption	30 μW
Power Supply	1.2 V & 3.0 V (2.1 V, −0.9 V)
Total Chip Area	1.5 mm × 1.0 mm
Communication Scheme	UWB @ 3.5 & 4.5 GHz
Unencoded Data Rate	100 kbps
Technology	TSMC 65-nm CMOS

Table 3.2: Performance Comparison of Wireless FSCV Microsystems

	This work	**[43]**	**[42]**	**[7]**
No. Channels	1	1	4	1
ADC Scheme	Nyquist	2^{nd}–ΣΔ	3^{rd}–ΣΔ	3^{rd}–ΣΔ
TX Scheme	IR-UWB	FSK	FSK	FSK
TX Data Rate	**Low**	High	High	High
Carrier Freq.	3.5-4.5 GHz	433 MHz	433 MHz	433 MHz
Power Supply	1.2, 3.0 V	±1.3 V	±1.25 V	−0.8, 1.7V
Sample Rate	10 kHz	10 kHz	10 kHz	10 kHz
Input Range	±430 nA	±430 nA	±750 nA	±950 nA
Input Noise	92 pA	132 pA	57 pA	55 pA
Bandwidth	2 kHz	5 kHz	5 kHz	5 kHz
Frontend Power	**14.4 μW**	57 μW	76 μW	9.3 μW
Transmit Power	**15.6 μW**	~1 mW	~1 mW	~0.4 mW
Total Power	**30 μW**	~1 mW	~1 mW	~0.4 mW
CMOS Node	65 nm	0.35 μm	0.35 μm	0.35 μm

3.6.1 Device Characterization

As described in Section 3.2, the core ADC does not digitize absolute input currents but rather resolves directly small input current differences relative to an arbitrary baseline current. To test the static linearity of the potentiostat and the core ADC, the input current was swept linearly in the range of ±10 nA in steps of 50 pA relative to a DC offset baseline current using a *Keithley* 236 DC current source. Figure 3.9 shows the measured output current for positive and negative baseline-subtracted input currents ranging from 50 pA to 10 nA.

3.6.2 Device Validation

For device validation with *in vitro* detection of dopamine, carbon fiber microelectrodes (CFMs) were fabricated as previously described in [27]. An individual carbon fiber with a 5-μm diameter was aspirated into a 1.8-mm glass capillary, which was heated and pulled on a micropipette puller. The exposed carbon fiber was cut to a length of ~150 μm under a microscope. Before use, the CFM was soaked in isopropanol purified with activated carbon for 15 minutes to remove surface impurities. The electrode was backfilled with a 150 mM KCl solution to promote electrical conduction. Ag/AgCl electrodes were used for both working and reference electrodes. The working electrode was inserted into the open end of the glass capillary.

An in-house flow injection analysis apparatus was used to validate the chip. The CFM and reference electrode were positioned at the inlet of a flow cell reservoir connected to the outlet of a two-position, six-port sample injector. All experiments were done in a buffer solution mimicking physiological ion concen-

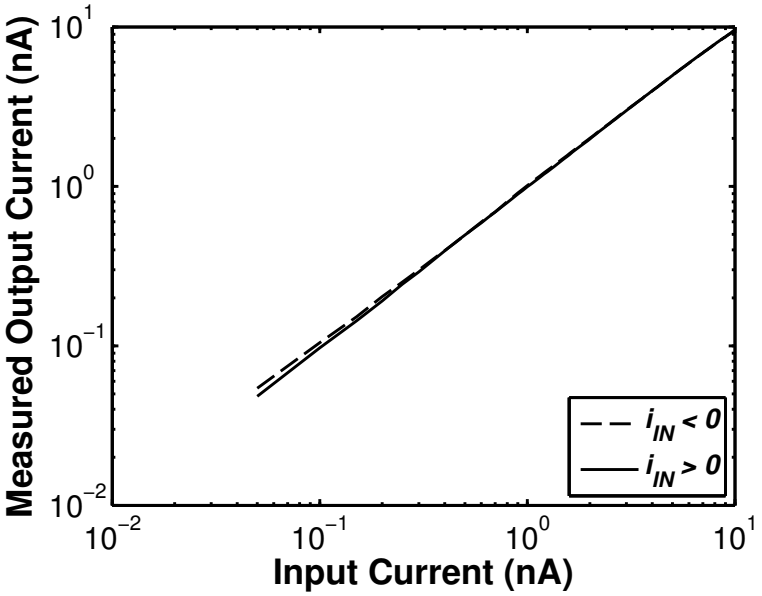

Figure 3.9: Measured static linearity of the potentiostat and A/D converter for positive and negative input currents in the range of 50 pA to 10 nA.

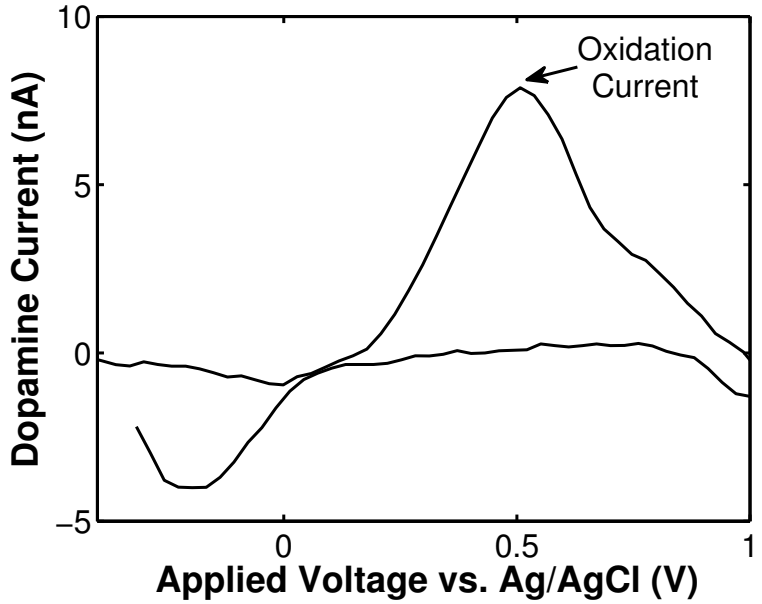

Figure 3.10: Background-subtracted cyclic voltammogram from a wireless recording of flow-injection of dopamine with a concentration level of 1 μM.

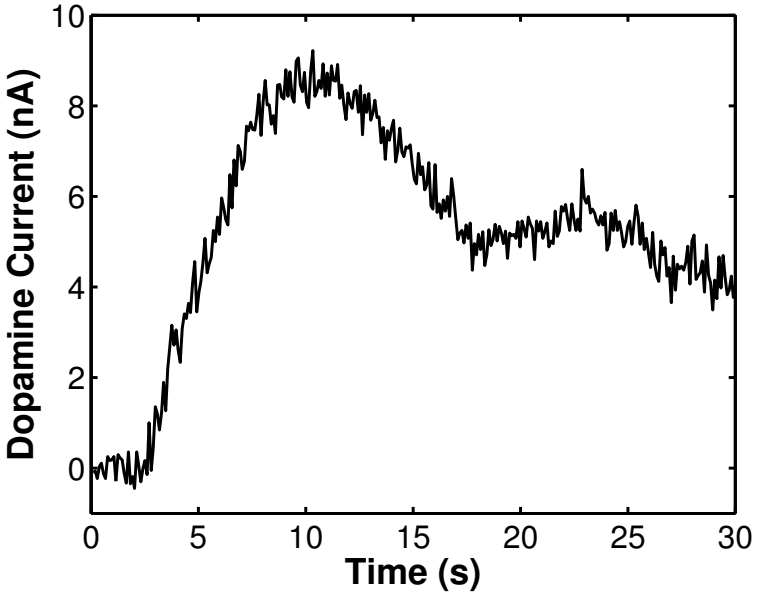

Figure 3.11: Time course of peak dopamine oxidation current from a wireless recording of flow-injection of a 250-μL bolus of 1-μM dopamine solution.

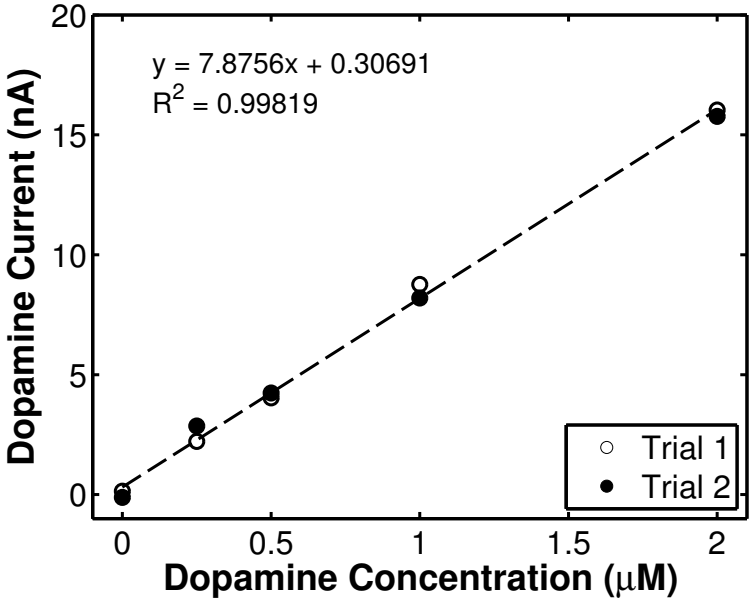

Figure 3.12: Calibration curve indicating peak oxidation current versus concentration, from wireless recordings of flow-injection of dopamine with concentration levels of 0 nM (buffer only), 250 nM, 500 nM, 1 μM, and 2 μM.

trations. The buffer solution contained 140 mM NaCl, 5 mM KCl, 2.5 mM $CaCl_2$, 1 mM $MgCl_2$, and 10 mM HEPES. NaOH was added to adjust the pH to 7.3. A 100 mM stock solution of dopamine, prepared on the same day of the experiments, was diluted in buffer solution to achieve concentration levels of 250 nM, 500 nM, 1 μM, and 2 μM. A syringe pump was used to introduce the buffer to the CFM at a flow rate of 1 mL/min. Before recording, consecutive 300-V/s, 10-Hz FSCV scans were applied to the CFM for 20 minutes to stabilize the electrode. The electrode voltage was swept from a resting value of −450 mV to a peak value of +1.05 V and back to its resting value in each scan. During recording, the sample injector was used to introduce a bolus of dopamine to the CFM. Background-subtracted dopamine signals were wirelessly recorded for all four concentrations. The CFM was kept immersed in the buffer solution during the entire recording session.

Figure 3.10 illustrates a background-subtracted voltammogram (average of 10 scans) obtained from a wireless recording of flow injection of dopamine with a concentration level of 1 μM. The peak currents around +0.5 V and −0.2 V vs. Ag/AgCl correspond to dopamine oxidation and reduction, respectively. Figure 3.11 illustrates the time course of the wirelessly-recorded dopamine oxidation current at +0.5 V (arrow in Figure 3.10) after injection of a 250-μL bolus of 1 μM dopamine solution at $t = 0$ seconds. The time course of the current reflects the dopamine concentration at the CFM. Figure 3.12 shows the calibration curve depicting measured dopamine oxidation current versus concentration. The data represent the mean of two independent wireless measurements for each concentration. In each trial, the mean is the average of 20 consecutive oxidation peaks starting at 8 seconds. The concentration dependence is linear with a sensitivity of 7.9 nA/μM. All ten *in vitro* measurements were wirelessly transmitted and

recorded at the receiver.

3.6.3 UWB Measurement Results

Figures 3.13–3.16 illustrate the measured performance of the UWB transmitter. Figure 3.13 depicts the measured output spectrum of the synchronization (sync) and data pulses at a pulse repetition rate of 100 kHz. Figure 3.14 illustrates the measured transmitted time-domain *sync* pulse signal with triangular pulse shaping. Figure 3.15 shows TX and RX timing signals indicating that the receiver can remain synchronized for at least up to 200 million cycles. Figure 3.16 shows the position of the prototype TX and RX antennas used for the wireless FSCV experiments, which were carried out inside a grounded Faraday cage to minimize electrical interference. The antennas were separated by a distance of 0.6 m while still achieving a bit error rate (BER) better than $5{\times}10^{-9}$.

3.7 Noise Analysis

In this section we present a noise analysis of the major noise contributors of the wireless FSCV system. For simplicity, we ignore the ADC's quantization noise as it is much smaller than the noise that appears at the input of the ADC during dopamine detection, which is predominantly input noise amplified by the potentiostat and MDAC stages. Figure 3.17 shows a circuit diagram of the sensing interface, i.e., potentiostat and MDAC, interfaced to the CFM. The CFM is modeled with a simplified Randles circuit comprised of the solution resistance R_S in series with the parallel combination of the charge-transfer resistance R_{ct}

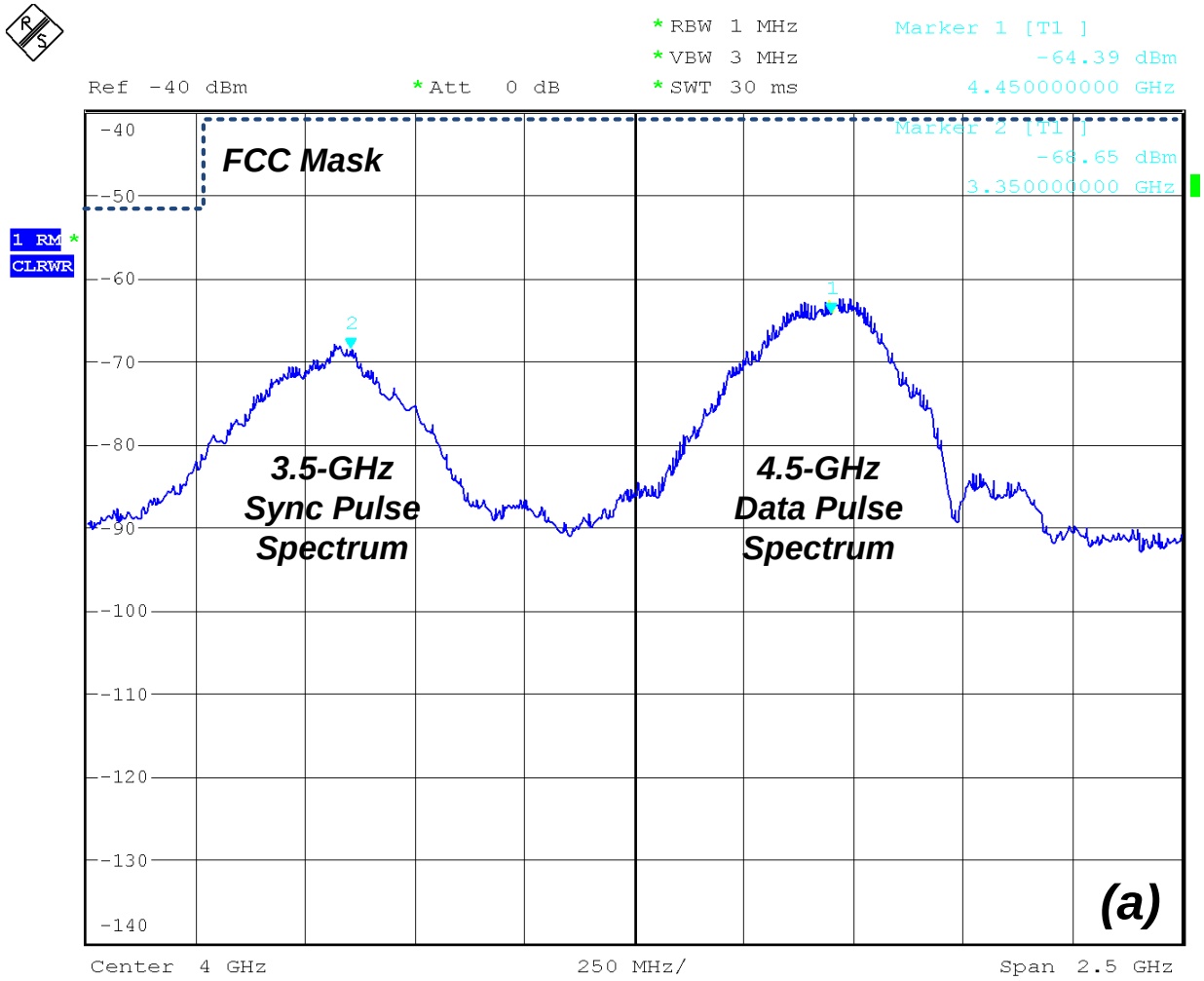

Figure 3.13: FCC-compliant spectrum of synchronization (*sync*) and OOK *data* pulses at a pulse repetition rate of 100 kHz.

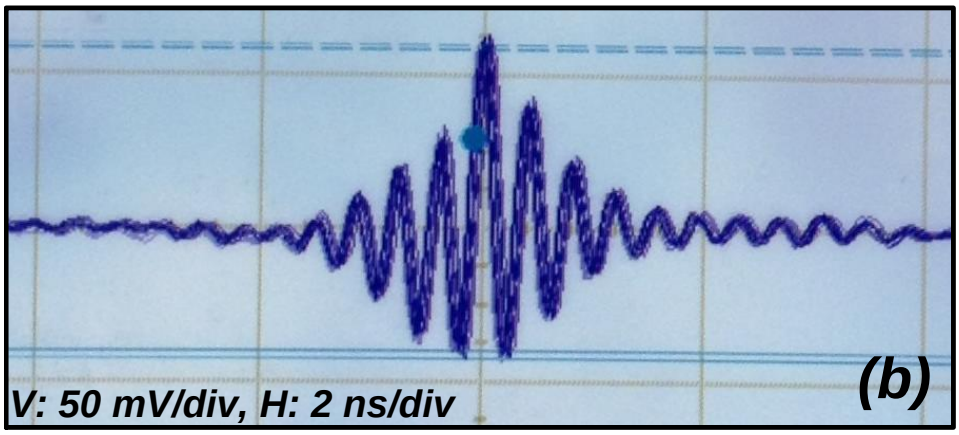

Figure 3.14: Time-domain *sync* pulse with triangle pulse shaping.

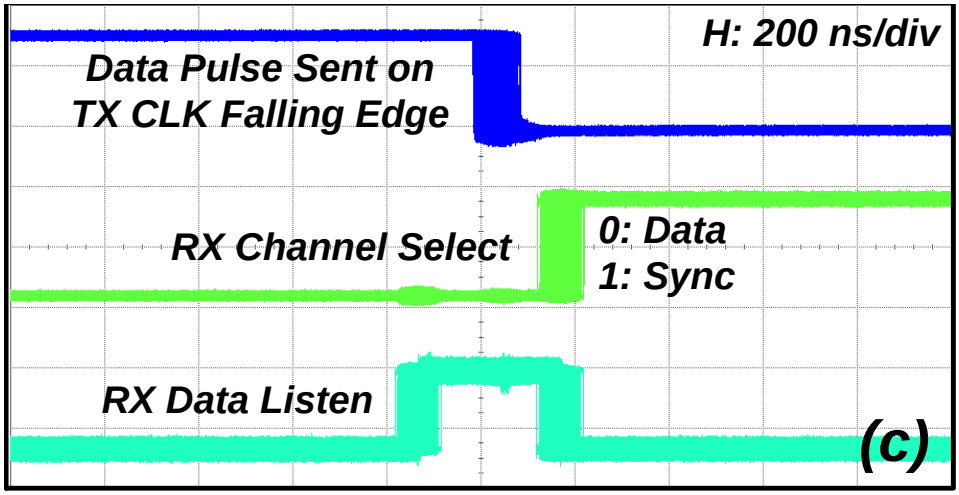

Figure 3.15: Synchronized receiver (RX) over 200+ million cycles.

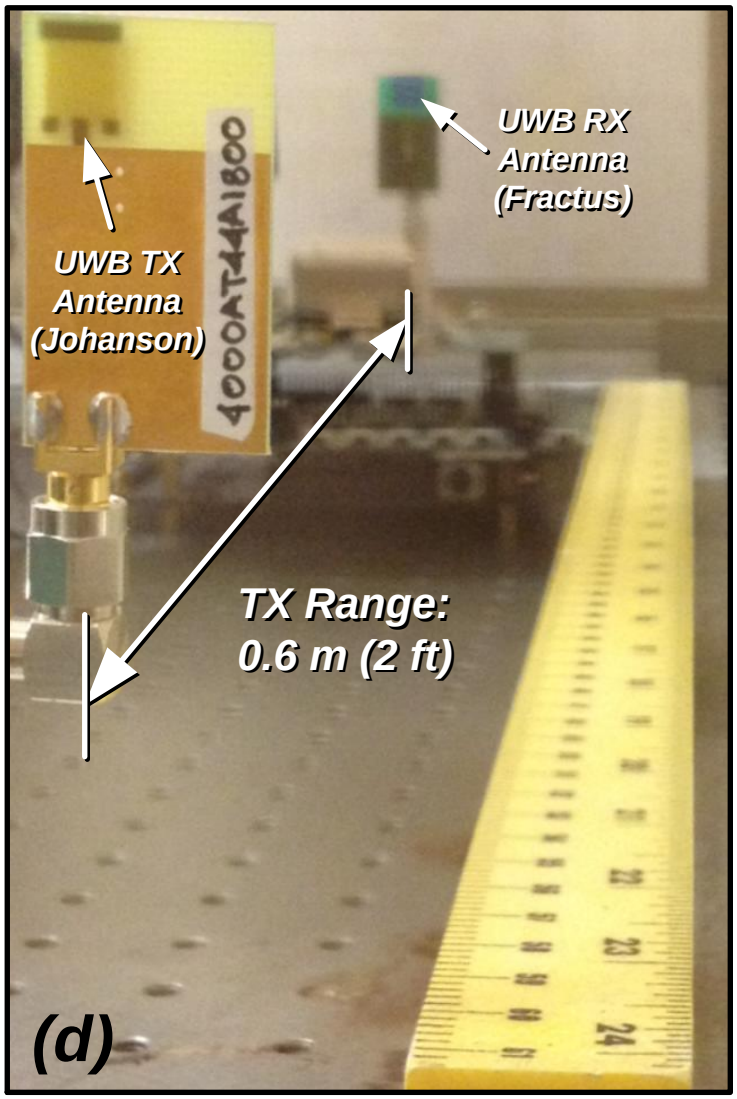

Figure 3.16: Antenna setup during wireless FSCV monitoring.

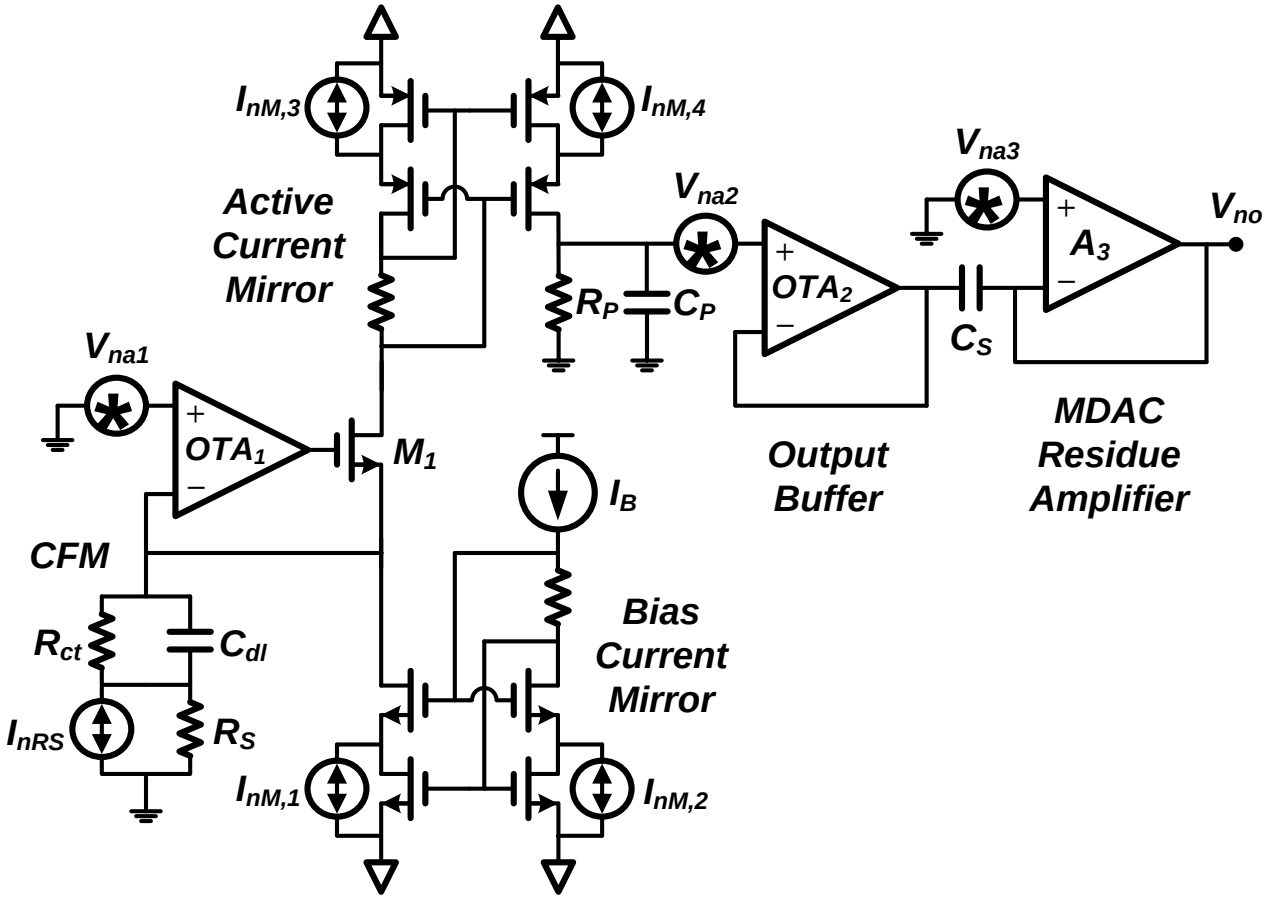

Figure 3.17: Schematic diagram illustrating the dominant noise sources in the sensing interface and carbon-fiber microelectrode (CFM).

and double-layer capacitance C_{dl} of the CFM. For the 150-μm CFM utilized in this work, values of R_S = 100 kΩ, R_{ct} = 100 MΩ, and C_{dl} = 1.5 nF were found to closely mimic the electrode's response during flow injection analysis, respectively. The circuit in Figure 3.17 has five dominant thermal noise sources: V_{na1}, V_{na2}, and V_{na3}, the equivalent input noise voltages of amplifiers OTA_1, OTA_2, and op-amp A_3, respectively; and I_{nRS} and I_{nM}, the noise currents of the solution resistance and the current mirror transistors, respectively. Their spectral densities are given by

$$\overline{V_{na1}^2} = 8kT\gamma g_{m1}^{-1}(1 + 3\, g_{m1,B}/g_{m1}) \tag{3.14a}$$

$$\overline{V_{na2}^2} = 8kT\gamma g_{m2}^{-1}(1 + 3\, g_{m2,B}/g_{m2}) \tag{3.14b}$$

$$\overline{V_{na3}^2} = 8kT\gamma g_{m3}^{-1}(1 + 3\, g_{m3,B}/g_{m3}) \tag{3.14c}$$

$$\overline{I_{nM}^2} = 16kT\gamma g_m \tag{3.14d}$$

$$\overline{I_{nRS}^2} = 4kTR_S^{-1} \tag{3.14e}$$

where K is the Boltzmann constant, T is the absolute temperature, $\gamma = 2/3$ is the thermal noise coefficient for long-channel devices, g_{m1-3} and $g_{m1-3,B}$ are the transconductances of the input and bias transistors of the amplifiers, respectively, and g_m is the transconductance of the current mirror transistors. We neglect $1/f$ noise in Equations 3.14a–3.14e due to the use of long channel lengths, i.e. 40 μm. Neglecting channel-length modulation and body effect, and assuming all noise sources are uncorrelated, the output noise spectral density $\overline{V_{no}^2}$ can be derived as Equation 3.15, where $\tau_z = R_{ct}C_{dl}$, $\tau_1 = R_S C_{dl}$, $\tau_2 = R_P C_P$, and τ_u is the inverse of the op-amp's unity-gain bandwidth. In the derivation of Equation 3.15, we have assumed OTA_1 is a wideband single-stage amplifier with a time constant $\tau_a \ll \tau_{1,2}$, and a high open-loop gain. Integrating Equation 3.15

$$\overline{V_{no}^2} \approx \frac{R_P^2}{R_{ct}^2}\left(R_S^2 \cdot \overline{I_{nRS}^2} + \overline{V_{na1}^2}\right)\left|\frac{1+s\tau_z}{(1+s\tau_1)(1+s\tau_2)}\right|^2 + R_P^2 \cdot \overline{I_{nM}^2}\left|\frac{1}{1+s\tau_2}\right|^2 + \left(\overline{V_{na2}^2} + \overline{V_{na3}^2}\right)\left|\frac{1}{1+s\tau_u}\right|^2 \tag{3.15}$$

$$\overline{I_{in,tot}^2} \approx \frac{1}{R_{ct}^2}\left(R_S^2 \cdot \overline{I_{nRS}^2} + \overline{V_{na1}^2}\right)\frac{1}{\tau_1+\tau_2}\left(1+\frac{\tau_z^2}{\tau_1\tau_2}\right)\frac{1}{4} + \overline{I_{nM}^2}\frac{1}{4\tau_2} + \left(\overline{V_{na2}^2} + \overline{V_{na3}^2}\right)\frac{1}{4\tau_u} \tag{3.16}$$

---

across $0 < f < \infty$, as derived in [38], and dividing by R_P^2 yields the total input-referred noise current, given by Equation 3.16. Applying Equations 3.14a–3.14e to Equation 3.16, plugging design values and taking the square root yields an input noise current of 89 pA_{rms} in a 2-kHz bandwidth, in excellent agreement with the measured value of 92 pA_{rms}. The last term in Equation 3.16, which represents the reset noise of the MDAC op-amp, is the limiting factor degrading noise performance due to the small τ_u required to achieve a fast settling time of 10 μs during the input S/H phase (φ_1).

3.8 Summary

In this chapter, we presented a 30-μW wireless microsystem for real-time *in vivo* monitoring of dopamine levels and a lightweight miniaturized device that can enable long-term behavioral studies in freely-behaving animals. On-chip integration of analog background subtraction and UWB telemetry yields a 32-fold increase in resolution versus standard Nyquist-rate conversion alone, near a four-fold decrease in the volume of uplink data versus single-bit, third-order,

delta-sigma modulation, and more than a 20-fold reduction in transmit power versus narrowband transmission for low data rates. We also demonstrated functionality of the system by wirelessly recording flow-injection of dopamine with concentrations in the range of 250 nM to 2 μM at a CFM using 300-V/s FSCV. Measurement results showed an input-referred RMS current noise of 92 pA and an input current range of ±430 nA at a conversion rate of 10 kHz. The system achieves low-power, low-data-rate impulse-based transmission of high-precision FSCV measurements without loss of salient data. To the best of the author's knowledge, the wireless microsystem and miniaturized device described in this chapter achieve the lowest power consumption among recently reported single-unit wireless microsystems [7,42,43] and miniaturized devices [35,41] for neurochemical monitoring using FSCV.

In the next chapter, we will present an electrochemical sensor array for high-throughput screening, another important application in neuroscience. We will describe a 1,024-electrode CMOS VLSI potentiostat array for massively-parallel electrochemical detection of transmitter release events from a large number of cells to accelerate the development and testing of drugs and treatments modulate many of the properties of neurotransmitter release events such as their size, frequency, and kinetics. We will also introduce a novel potentiostat topology capable of measuring bidirectional input currents from redox processes with high precision to enable not only amperometry but also FSCV using planar microfabricated electrode arrays.

CHAPTER 4

A 32 × 32 CMOS VLSI POTENTIOSTAT ARRAY FOR MASSIVELY-PARALLEL NEUROCHEMICAL MONITORING USING FAST-SCAN CYCLIC VOLTAMMETRY

4.1 Introduction

Nerve cells, i.e., neurons, are the basic processing unit of the nervous system. Neurons communicate with each other via a chemical signaling process mediated by the storage and release of neurotransmitters, a set of biomolecules that act as chemical messengers to regulate neuronal function and behavior [46]. Neurons store high concentrations of these biomolecules in small membrane-bound secretory vesicles attached to the inside of the presynaptic plasma membrane. When the presynaptic terminal is electrically stimulated, the vesicles fuse with the plasma membrane of the neuron through a process known as exocytosis, releasing the vesicle contents into extracellular space [33]. Transmitter release from a single vesicle is known as quantal release, and the number of biomolecules expelled in a quantal release event is termed the quantal size [15]. Quantal release has been the subject of extensive medical research since some of the underlying mechanisms mediating exocytosis, such as vesicle pore fusion, are still not fully understood. A better understanding of properties such as the quantal size as well the frequency and time course of quantal events is necessary for the discovery and development of new therapeutic drugs that modulate these properties.

Several recording techniques have been used to investigate the properties of quantal release events and their modulation. The two most prevalent tech-

niques are constant-potential amperometry [10, 49] and fast-scan cyclic voltammetry (FSCV) [5, 50] at a polarizable working electrode. Traditionally, a carbon fiber microelectrode (CFM) has been used as the working electrode due its chemically inert properties, small dimensions, i.e., ~5–20 μm diameter, and thus fast response time [22].

In carbon-fiber amperometry, the CFM working electrode is held at a positive potential with respect to a silver/silver-chloride (Ag|AgCl) reference electrode, typically ~600-700 mV. Neurotransmitters and hormones from the catecholamine family, such as dopamine and its conversion products adrenaline and noradrenaline, easily oxidize when they come in contact with the surface of the CFM, releasing two electrons each in the process [5]. The resulting electron transfer is then measured as a transient current. Thus, a single exocytotic event such as catecholamine release from chromaffin cells or dopamine release from dopaminergic neurons can be measured as an amperometric current spike, with high precision and high temporal resolution using carbon-fiber amperometry. Integration of the transient current spike yields the total charge, from which quantal size can be calculated.

In FSCV at a CFM, the voltage at the working electrode is swept linearly from an initial value of −0.5 V to peak value of +1.0 V within 5 ms and back to the initial value over the next 5 ms. These long 10-ms sweeps, or scans, are repeated every 100 ms. The fast rate at which the voltage changes, or the high scan rate, gives rise to a large background current on which the small *faradaic* current due to oxidation and reduction of an electroactive compound is superimposed [40]. To recover the *faradaic* current, the background current elicited during the absence of the compound is subtracted from the total current (sum

of background and *faradaic* currents) elicited during the presence of the compound through a procedure known as background subtraction [25]. This *faradaic* component is then plotted versus the applied voltage to yield a background-subtracted voltammogram from which the oxidation and reduction voltages can be extracted to identify the detected compound.

However, carbon-fiber recordings have their limitations. In particular, the technique is only capable of measuring quantal release events from one cell at a time. Each single-cell experiment is time-consuming and laborious, requiring precise manual positioning of the CFM adjacent to an individual cell that releases neurotransmitters. Thus, carbon-fiber recordings are not suitable for drug screening, a process that requires a statistically significant set of measurements from a large number of cells to obtain conclusive evidence on the effect of a drug on quantal release.

Microelectrode arrays (MEAs) have recently emerged as a viable candidate to replace CFMs as the working electrode mainly because the microfabrication and surface modification techniques involved in the production of MEAs not only provide better reproducibility than traditional CFM fabrication methods but also facilitate batch fabrication of the electrodes [52, 53]. Surface-patterned planar MEAs using noble metals such as gold and platinum have recently been applied to measure quantal release events from single cells [2, 6, 24, 51]. Amperommetry and FSCV using MEAs have recently been demonstrated in [34, 54]. Amperometry using MEAs allows the simultaneous recording of quantal release events from a large number of cells. FSCV using MEAs serves as a complimentary technique that allows the simultaneous identification of multiple secreted compounds across different types of cells [26]. The latter tech-

nique is also useful to perform batch impedance characterization of surface-patterned electrodes by comparing voltammograms obtained using a redox reporter biomolecule against a known standard [17].

This chapter describes a 32×32 (1,024 electrode) CMOS VLSI potentiostat array for high-throughput amperometric and voltammetric recording of quantal release events to accelerate the development and testing of new treatments that modulate the size and kinetics of quantal release. The potentiostat array provides a ten-fold increase in the number of measuring electrodes and a five-fold increase in temporal resolution over the previous design we reported in [34]. The array employs a novel potentiostat circuit topology capable of measuring bidirectional input currents from redox processes with high precision.

4.2 System Architecture

Figure 4.1 illustrates the system architecture of the 32×32 potentiostat array with on-chip working electrodes. The array consists of a set of 16 identical read-out columns along with on-chip biasing and timing circuit blocks, as shown in Figure 4.1(a). Each read-out column contains a set of 64 detectors laid out as a 32×2 sub-array, as shown in Figure 4.1(b). The detectors share a common output stage similar to that described in [3]. The output stage consists of a correlated double sampling (CDS) circuit connected to a unity-gain output buffer. The CDS circuit provides $1/f$ noise and offset cancellation. The output buffer provides a low output impedance to ensure reliable read-out at a sampling rate of 640 kS/s. The detectors in each read-out column are switched sequentially via a set of select signals from the timing block using a time-division multiplexing

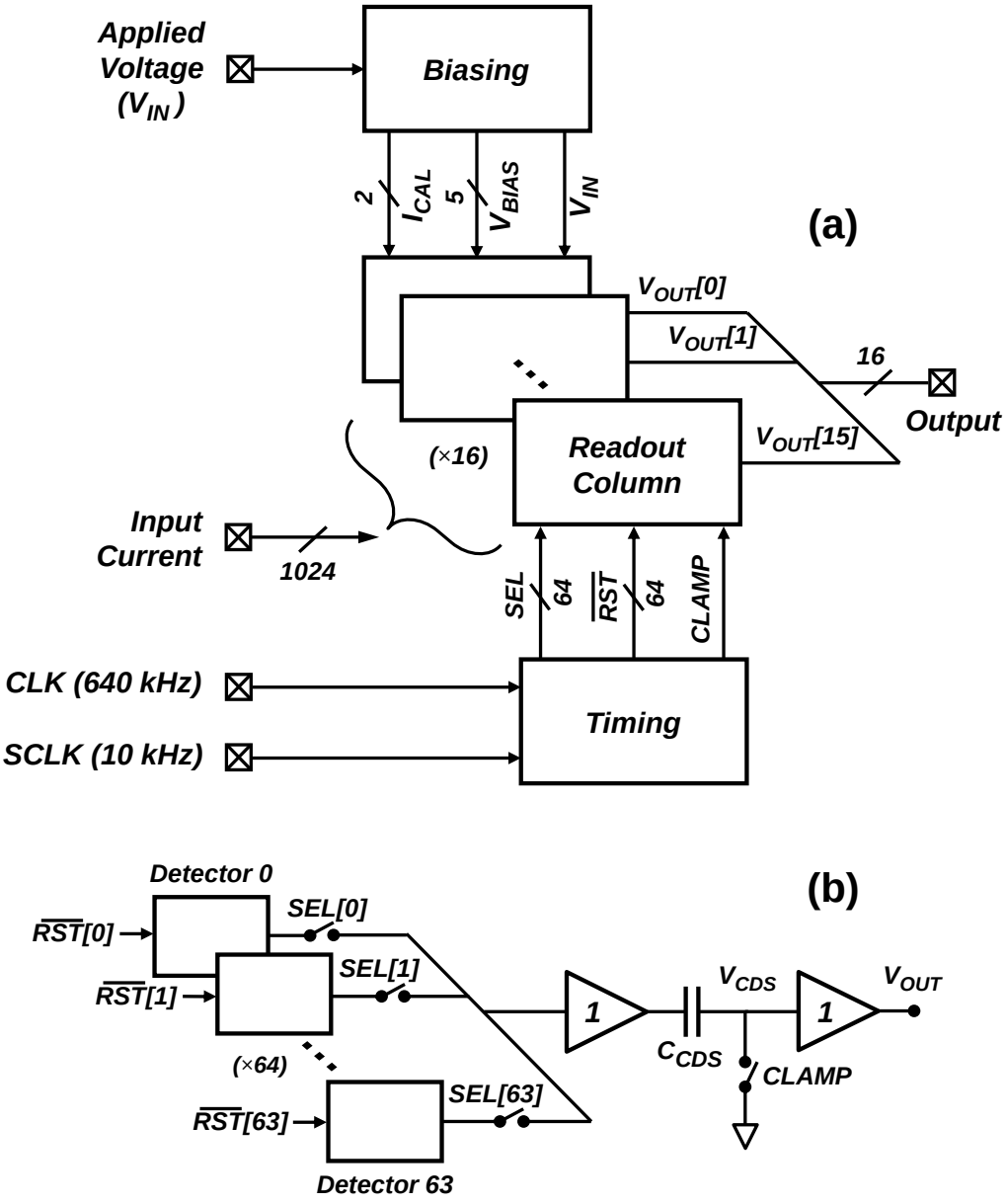

Figure 4.1: System-level diagram of the 32 × 32 CMOS VLSI bidirectional-current electrochemical detector array. (a) The system consists of 16 identical read-out columns along with on-chip biasing and timing blocks. (b) Each read-out column contains 64 detectors that share a common output stage consisting of a correlated double sampling (CDS) circuit and an output buffer. Detectors in each read-out column are switched sequentially using a time-division multiplexing technique.

technique described in detail in Section 4.3. The output from each read-out column is then fed to one channel of an external multi-channel A/D converter for acquisition.

4.3 Circuit Implementation

4.3.1 Bidirectional-Current Electrochemical Detector

Traditional unidirectional-current electrochemical detectors such as the one described in [21] use a DC offset current to measure bidirectional currents, which not only adds noise (but does not provide gain) to the signal path but also disturbs the charge balance of the electrode-electrolyte interface [30]. The core of the electrochemical detector array described here is a novel potentiostat circuit capable of measuring bidirectional currents from both oxidation as well as reduction process without the use of a DC offset current. This bidirectional-current detection feature enables not only constant-potential amperometry but also FSCV.

Figure 4.2 shows the schematic diagram of a single potentiostat unit, which operates as follows. A reset signal $\overline{RST}$ is initially asserted to precharge node V_{INT} to V_{DD} through the PMOS switch S_1. After the reset signal is de-asserted, node V_{INT} is discharged with the input current through one of two branches for a period of 100 μs. For positive input currents ($i_{IN} > 0$), which are generally present during the positive slope of the voltage ramp, the circuit operates as the regulated cascode amplifier (RCA) described in [3], with cascode transistor M_1 and regulation amplifier A_1 turned on. In this case, the input current i_{IN} flows

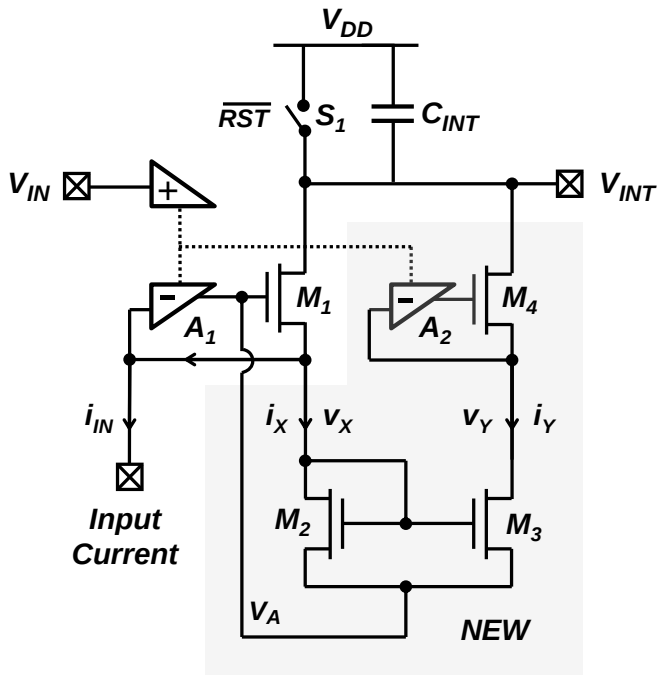

Figure 4.2: Schematic diagram of the improved bidirectional-current electrochemical detector unit. The potentiostat acts as a regulated cascode amplifier for positive input currents, and as an active-input regulated cascode mirror for negative input currents.

directly through M_1 out of a 50-fF capacitor C_{INT} into the electrolyte, producing an integration voltage given by

$$V_{INT} = V_{DD} - \frac{1}{C_{INT}} \int_0^{T_0} i_{IN}(t)\, dt, \tag{4.1}$$

where T_0 is the period of the integration phase. For the negative input currents ($i_{IN} < 0$) that occur during the negative slope of the voltage ramp, transistor M_1 shuts off and the circuit operates instead as an active-input regulated-cascode current mirror [44], with regulation amplifiers A_1 and A_2 as well as current-mirror transistors M_2 and M_3 and cascode transistor M_4 turned on. Since M_1 is off in this case, the input current flows through branch i_X and is mirrored onto branch i_Y with high precision, producing an integration voltage identical

to Equation 4.1. The negative feedback loops in the two RCA circuits ensure the drain voltages v_X and v_Y of the current mirror not only are equal to each other but also track accurately the applied voltage V_{IN}, forcing the current i_Y to be identical to i_X across a wide-range of applied voltages. The active-input regulated cascode mirror topology achieves superior accuracy compared to the active-input current mirror described in [45], which suffers from systematic errors due to channel-length modulation effects, and to the low-current regulated cascode mirror described in [30, 55], whose accuracy depends on process and circuit parameters due to the use of single-input regulating amplifiers. The improved potentiostat could be implemented at the cost of only six additional transistors compared to the original potentiostat in [3], because A_2 was conveniently designed as a half amplifier to take advantage of the shared amplifier scheme described in [3] to minimize the transistor count per detector. The potentiostat also avoids use of two separate PMOS and NMOS integration stages [37], which increase the real estate of the detector.

4.3.2 Timing Block

Given the large number of detectors in the array, time-division multiplexing was implemented to reduce the number of outputs to be sampled off-chip. Although multiplexing the outputs of all 1,024 detectors into a single output line was a possibility, we limited the number of multiplexed outputs per output line to 64 to avoid the use of a high-frequency on-chip clock, which would add excessive switching noise. Figure 4.3 shows the timing scheme used to implement time-division multiplexing of the 64 detectors in each read-out column. Figure 4.3(a) shows a schematic diagram of the timing block, which consists of a 64-stage

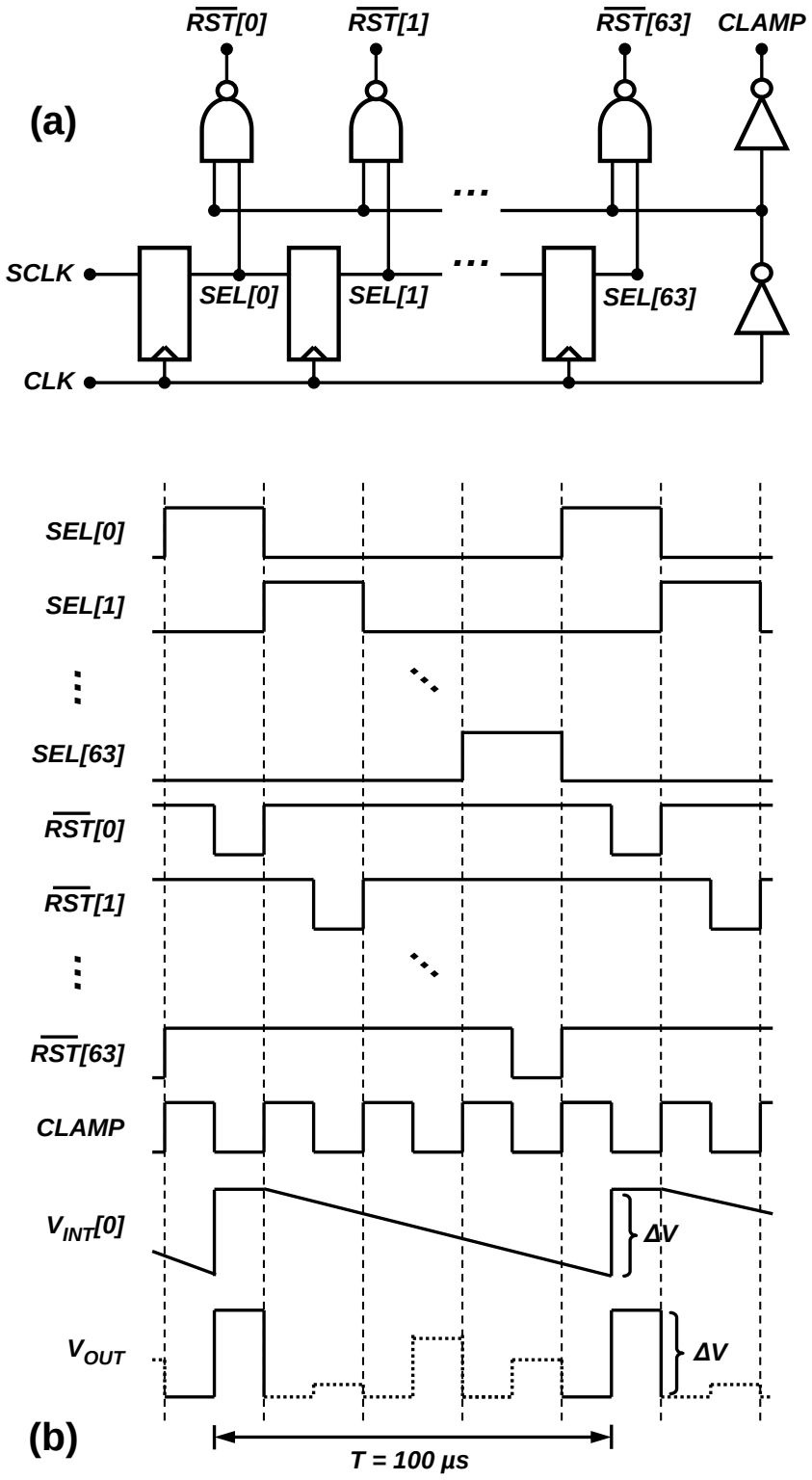

Figure 4.3: Timing scheme used to implement time-division multiplexing in each column: (a) timing circuit and (b) timing signals.

shift register along with minimal combinational logic. Figure 4.3(b) shows the corresponding timing signals produced by the timing block. The shift register is driven by two external clocks: a 640-kHz main clock, *CLK*, with 50% duty cycle and a 10-kHz shift clock, *SCLK*, with ~1% duty cycle. *SCLK* is pulsed high briefly every 100 μs. At the positive edge of the main clock, the output of the first *D* flip flop, *SEL[0]*, goes high to select the output of one of the 64 detectors in each of the 16 parallel read-out columns for one period of the main clock. Consecutive positive edges of the clock activate select signals *SEL[1]* through *SEL[63]* in a sequential manner, as seen in Figure 4.3(b). The process is repeated with each consecutive *SCLK* pulse. A set of NAND gates is used to derive reset signals $\overline{RST}$*[0]* through $\overline{RST}$*[63]* to reset one detector at a time for half of a main clock period. A buffer is used to derive the clamping signal, *CLAMP*, which is fed to the CDS block in each of the 16 parallel read-out columns.

4.3.3 Correlated Double Sampling Circuit

The CDS block operates as follows. At the end of the integration period for a particular detector, e.g., Detector 0, select signals *SEL[0]* and *CLAMP* are asserted, as shown in Figure 4.3(b). *SEL[0]* connects the detector's output, i.e., V_{INT}*[0]*, to the left plate of capacitor C_{CDS} while *CLAMP* grounds the right plate, as depicted in Figure 4.1(b). Thus, the voltage across capacitor C_{CDS} at the end of the integration period is equal to Equation 4.1. At the onset of reset, *CLAMP* is de-asserted first and $\overline{RST}$*[0]* is subsequently asserted (pulsed low). During this time, the left plate of the capacitor C_{CDS} is pulled to V_{DD} while the right plate is left floating. Subtracting V_{INT}, i.e., the voltage previously stored across capacitor C_{CDS}, from V_{DD} yields

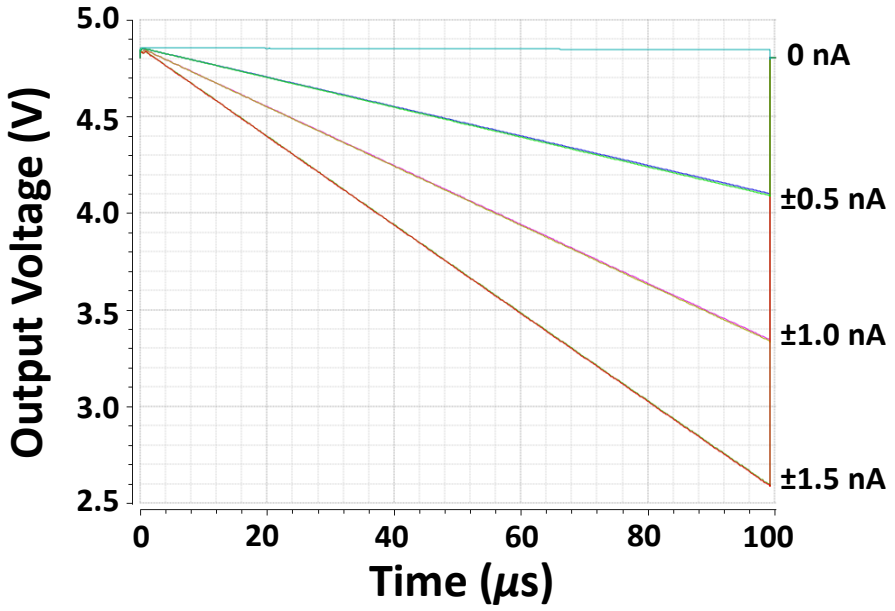

Figure 4.4: Linearity of the new potentiostat circuit obtained from simulation. The output voltage varies linearly with bidirectional input currents in the range of ±1.5 nA.

$$V_{OUT} = V_{CDS} = \frac{1}{C_{INT}} \int_0^{T_0} i_{IN}(t)\, dt \equiv \Delta V, \tag{4.2}$$

where V_{OUT} and V_{CDS} are the outputs of the read-out column's common output buffer and shared CDS block, respectively, as seen in Figure 4.1(b), and ΔV represents the voltage step in the signal V_{OUT} shown in Figure 4.3(b).

4.4 Simulation-Based Studies

4.4.1 Potentiostat

The performance of the bidirectional-current potentiostat was initially assessed using the Spectre simulator from Cadence Systems. To test the linearity of the potentiostat, the input current was swept parametrically in the range of ±1.5 nA in steps of 500 pA. Figure 4.4 illustrates the simulated time-domain response of the potentiostat over a 100-μs integration period. The potentiostat's output voltage, V_{INT}, decreases linearly with time for all of the DC input current values in the parametric set. Also, the magnitude of the integration slope increases linearly with input current. In addition, high matching accuracy is evidenced by the indistinguishable superimposed traces corresponding to the positive and negative values of a given input current magnitude, e.g., ±1.5 nA.

4.4.2 Read-Out Column

To examine the performance of the circuit in a simulation for a current waveform as expected for FSCV, a current signal measured with a carbon fiber microelectrode (CFM) was generated. In this measurement, a voltage ramp increasing from −0.45 V to +1.0 V over 50 ms (i.e., scan rate 29 V/s) and back to −0.45 V over the next 50 ms, was applied (Fig. 4.5(a)). Using a simple flow system, the CFM current was first measured in the absence of dopamine (DA) (Fig. 4.5(b), grey line), followed by a measurement in the presence of 2 μM DA (Fig. 4.5(b), black line). In the simulation, the voltage sweep shown in Figure 4.5(a) was used as the applied voltage (V_{IN}) for all 64 detectors in one read-out column and

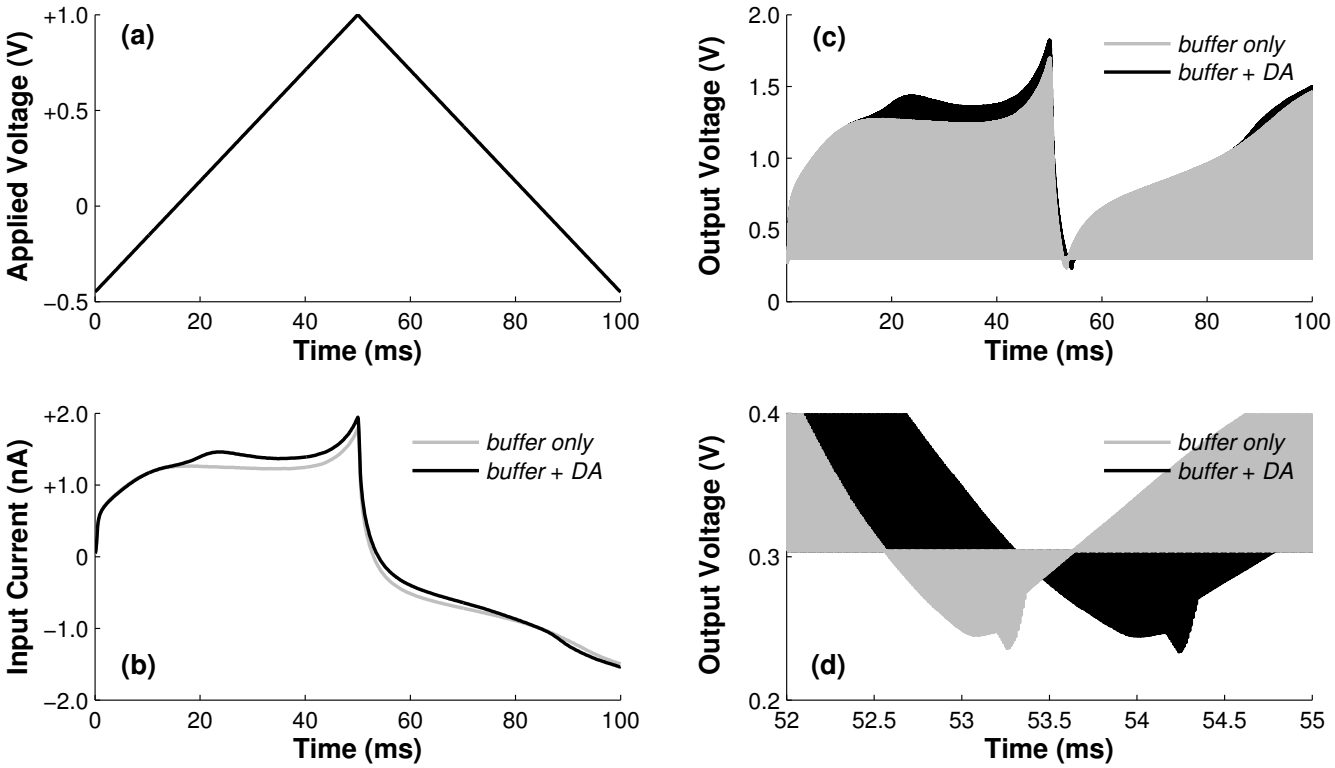

Figure 4.5: Simulation results for the read-out column. (a) Applied voltage and (b) input current from a 2 μM dopamine (DA) recording. (c) The envelope of the output encodes the absolute value of the input current. (d) The slope of this envelope changes sign but retains the same magnitude at the zero-crossings of the input current at $t = 53$ and $t = 54$ ms. Identification of these sharp V-shaped turns is key to recover negative values of the current.

the measured currents (Fig. 4.5(b)) as corresponding input currents (i_{IN}). The slower scan rate compared to the standard 300 V/s FSCV was chosen to prevent saturation of the high gain amplifier of the array. However, this scan rate is sufficient for on-chip electrode impedance characterization. Figure 4.5(c) shows the simulated time-domain response of the read-out column's multiplexed output V_{OUT} for both input current stimuli.

It is evident that the potentiostat topology used in this work does not measure the input current directly but rather provides the absolute value of the current, which is then encoded in the envelope of the output by the multiplexing scheme. This behavior is due to the use of the same integration stage for both positive and negative input currents. To recover the original input current, sign inversion of the negative values of the current was performed offline as follows. First, the zero crossings of the two input current stimuli were identified through visual inspection by leveraging the fact that the slope of the absolute value of a signal, e.g., the absolute value of the input current encoded in the envelope of the output, changes sign abruptly but retains the same magnitude at the zero crossings of the input current. The basic idea behind this concept is illustrated in Figure 4.5(d). With this method, zero crossings at t = 53 ms and t = 54 ms were found for the two input current stimuli as evidenced by the sharp V-shaped turn of the envelope of the outputs in Figure 4.5(c) around these times, respectively. Second, *a priori* knowledge of the shape of the current expected for FSCV was used to confirm that only those values to the right of the zero crossings were the ones that needed sign inversion.

Figure 4.6(a) shows the voltammograms obtained for the currents measured in the absence of DA (grey line) and in the presence of DA (black line), after

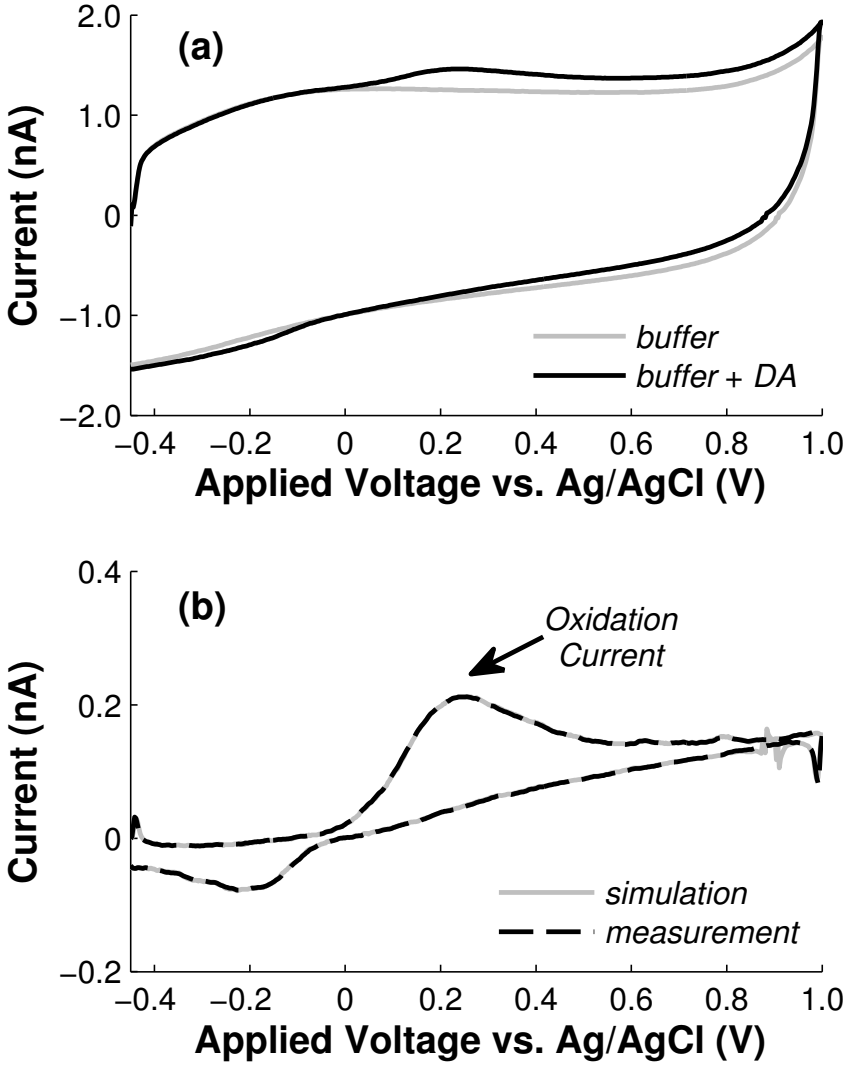

Figure 4.6: (a) Simulated background voltammograms before (*buffer*) and after (*buffer + DA*) dopamine (DA) injection. (b) Background-subtracted cyclic voltammograms obtained from the measured input current stimuli in Fig. 4.5(b) (*measurement*) and the simulated outputs in Fig. 4.6(a) (*simulation*).

demultiplexing, sign inversion, gain normalization, offset correction, and time shifting (in that order) of the two outputs in Figure 4.5(c). A time shift of 50 μs was used to correct for the intrinsic time lag, equal to half of an integration period, produced during integration of the piecewise linear inputs. Figure 4.6(b) shows the background-subtracted voltammograms obtained from both the measured input currents (*measurement* trace) in Figure 4.5(b) as well as the simulated outputs (*simulation* trace) in Figure 4.6(a). The detector measures with high accuracy all input current values in the range of ±2 nA as evidenced by the indistinguishable superimposed *measurement* and *simulation* traces in Figure 4.6(c), except for those values near the zero crossings of the input current, as seen by the small excursions near +0.9 V. However, these small deviations have a negligible effect on the voltammogram as they occur at a non-critical applied voltage, far from the critical oxidation and reduction peaks of interest observed near +0.25 V and −0.2 V, respectively.

4.5 Preliminary Results

Figure 4.7 shows a micrograph of the CMOS IC, which was fabricated in ON Semiconductor's 0.5-μm technology. Each potentiostat unit includes a 10 μm × 10 μm glass cut for post-CMOS surface-patterning of the electrode, and operates within the typical electrode voltage range of −0.5 V to +1.5 V (vs. Ag/AgCl) for FSCV, at a maximum scan rate of 30 V/s. The area of each potentiostat is 45 μm × 30 μm. The total area of the array is 1.5 mm × 1.0 mm for 1,024 elements. Each read-out column draws 0.5 mA from a 5-V supply, yielding a total power consumption of 40 mW for the entire array. Further measurements are needed to characterize and validate the fabricated chip. However, several challenges

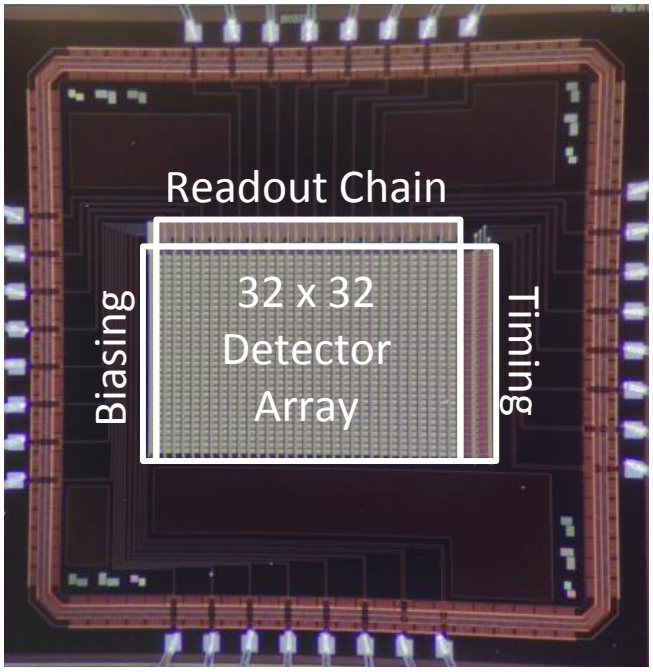

Figure 4.7: Micrograph of the fabricated detector array chip.

encountered during testing prevented the collection of these measurements at the time of writing. It is believed that excessive leakage current from the very large ESD protection structures, i.e., diode clamps, in the pads used in this work (borrowed from a pad collection for digital circuits) is affecting critical sensitive analog nodes in the biasing block, resulting in improper operation of the chip. At the time of writing, a small section of the array, i.e, a single read-out channel with 64 detectors, was sent for fabrication with bare pads instead, i.e., no ESD protection devices in the pads, to test this hypothesis.

4.6 Discussion

As mentioned previously in Section 4.4, the bidirectional-current detector does not measure input currents directly but rather provides the absolute value in-

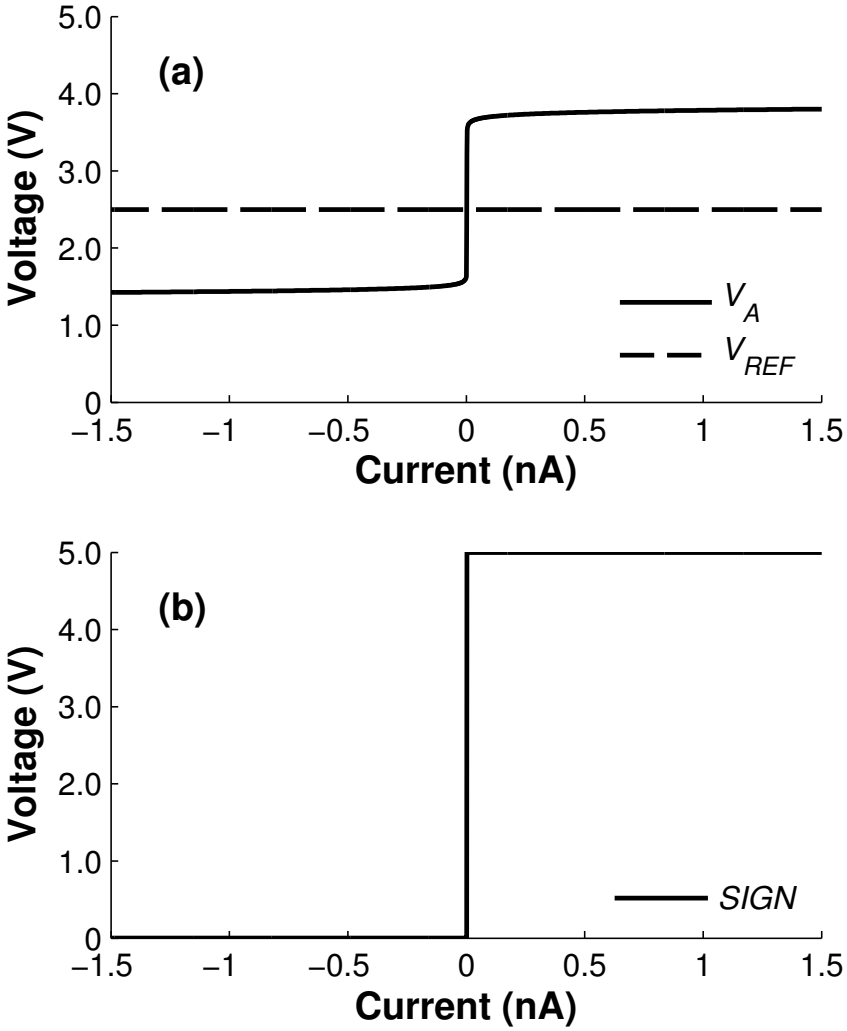

Figure 4.8: Simulation results illustrating the signals used to generate a binary output signal corresponding to the sign of the current. (a) The output of the regulation amplifier A_1 in Figure 4.2, i.e., node V_A, is pulled several hundred millivolts higher and lower than the applied voltage V_{REF} for positive and negative input currents, respectively. (b) The two signals in (a) can be fed to the comparator in Figure 4.9 to generate the desired binary output signal *SIGN*.

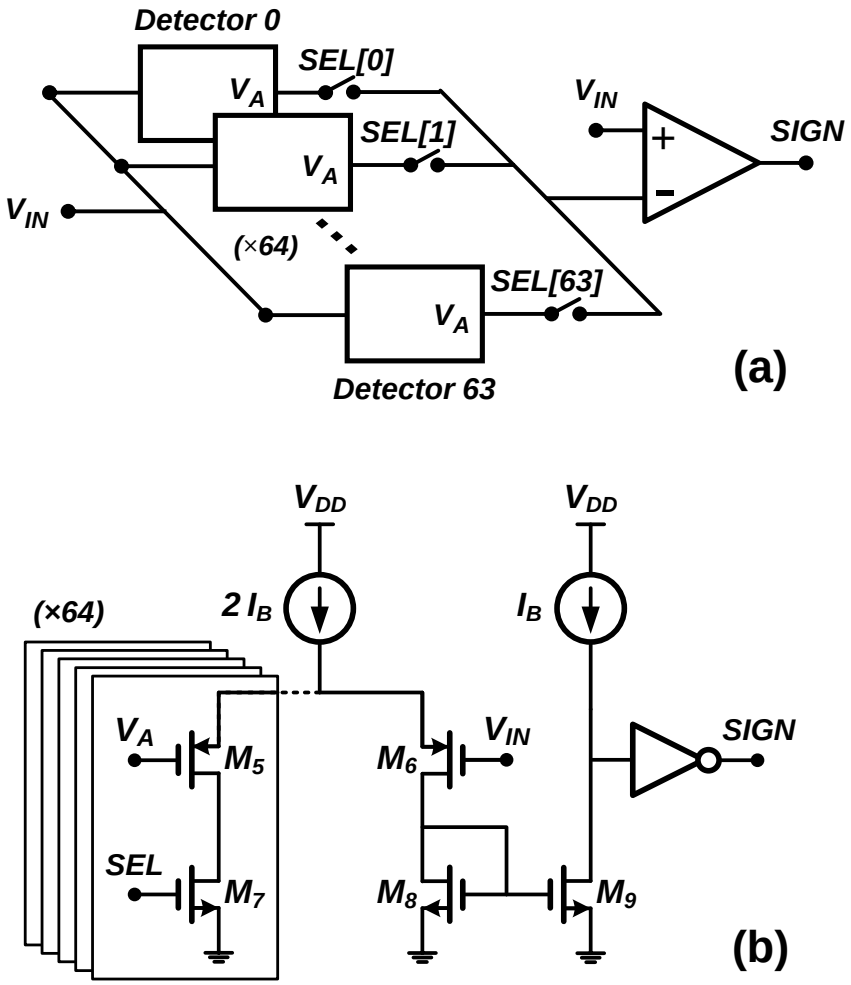

Figure 4.9: (a) Proposed modification to each read-out column in the array to generate a binary output signal corresponding to the sign of the input current. (b) Proposed implementation of the shared comparator shown in (a). The proposed solution only adds two additional transistors and a read-out line per detector for a negligible increase in detector area.

stead due to the use of the same integration stage for both negative and positive currents. In this work, the negative currents were recovered via manual sign inversion during offline analysis. The process was effective given that an identical input current was applied to all the detectors in a read-out column during the simulation. In reality, the input current will vary considerably from detector to detector during actual measurements. Thus, manual sign inversion becomes impractical for analyzing measurements from all of the 1,024 detectors in this array. In this case, implementing a zero-crossing detection algorithm using the rules described in Section 4.4 becomes necessary, although not sufficient because the algorithm could miss, in theory, some crossings in the presence of noise. A more holistic approach to solve this issue involves generating a binary output signal that reflects the sign of the input current in each detector.

One such implementation, which requires only a minor modification to the existing circuitry, leverages the fact that the output of the regulation amplifier A_1 in Figure 4.2, i.e., node V_A, is pulled several hundred millivolts higher and lower than the applied voltage V_{IN} for positive and negative input currents, respectively, as illustrated in Figure 4.8(a). Figure 4.9(a) shows the proposed modification for generating the binary output signal *SIGN* depicted in Figure 4.8(b). The technique takes advantage of the same time-division multiplexing and shared-amplifier schemes described in Section 4.2. When the select signal for a particular detector, e.g., Detector 0, goes high for one period of the main clock, a comparator shared by all detectors in a read-out column, compares V_{IN} versus the V_A node of that particular detector. Figure 4.9(b) shows a simplified schematic diagram of the shared comparator, which operates as follows. For negative input currents, V_A becomes lower than V_{IN} and all of the input current flows into the detector through the PMOS transistor M_5 and the NMOS

switch M_7. Thus, the drain voltage of NMOS transistor M_9 is pulled to V_{DD}, which forces the digital output signal *SIGN* to go low (Fig. 4.8(b)). Similarly, for positive input currents, V_A becomes higher than V_{IN} and all of the input current flows instead into the common NMOS current mirror formed by M_8–M_9 through PMOS transistor M_6. Thus, the drain voltage of M_9 is pulled to ground instead, which forces the *SIGN* to go high (Fig. 4.8(b)). The proposed scheme only requires two additional transistors, i.e., M_5 and M_7, and an extra read-out line per detector, yielding a negligible increase in detector area.

4.7 Summary

In this chapter, we presented a scalable 32 × 32 (1,024-electrode) CMOS VLSI potentiostat array for high-throughput screening applications and introduced a novel potentiostat circuit topology for application of bipolar voltages and high precision measurements of bidirectional currents. The proposed circuit enables not only amperometry but also FSCV at a MEA for massively-parallel detection of quantal release events and characterization of electrode impedance, respectively. We demonstrated functionality of the system through simulation-based studies using input stimuli obtained from actual recordings. We discussed the potentiostat's inability to detect the sign of the current, established a methodology for recovering the negative values of the current via a sign inversion procedure, and suggested a minor circuit modification to capture the sign of the current via a binary output signal with minimal area overhead.

CHAPTER 5

CONCLUSION AND FUTURE DIRECTIONS

In this dissertation, microsystems that incorporate the neurochemical monitoring technique fast-scan cyclic voltammetry (FSCV) were developed. These microsystems advance the current state of neuroscience by enabling two important applications: long-term monitoring in freely behaving animals to elucidate the intricate relationship between dopamine release and behavior, and high throughput screening to accelerate the development and testing of drugs and treatments that modulate transmitter release.

5.1 Contributions

Several contributions to the field of neuroscience field have been made in this research work. First, FSCV was introduced as a powerful neurochemical monitoring tool that, contrary to other methods such as amperometry, allows not only identification of neurochemicals but also characterization of electrode impedance. Second, a dynamic range enhancement technique termed analog background subtraction was introduced to reduce the wireless data rate requirement of integrated neurochemical monitoring systems by discarding redundant background information before wireless transmission. A rigorous theoretical analysis of the technique was provided, and its performance against other dynamic range enhancement techniques such as sigma-delta modulation was evaluated. Third, a two-step cyclic ADC architecture was developed to implement analog background subtraction on-chip with very low power consumption, and the system was thoroughly validated with flow-injection analysis experiments. Fourth, UWB telemetry was introduced as a promising candidate for low-data-

rate monitoring applications, and its performance against other transmission schemes such as narrowband communication was assessed. Fourth, a fully-integrated wireless microsystem incorporating analog background subtraction with UWB telemetry was developed to achieve ultra-low-power wireless transmission of high-precision FSCV measurements without any loss of salient data. On-chip integration of these two techniques yielded a 32-fold increase in resolution versus standard Nyquist-rate conversion alone and near a four-fold decrease in the volume of uplink data versus single-bit, third-order, delta-sigma modulation, and more than a 20-fold reduction in transmit power versus narrowband transmission at low data rates. The system was also thoroughly validated with wirelessly-recorded flow-injection analysis experiments. Fifth, a lightweight miniaturized wireless device was developed to enable long-term monitoring studies in freely-behaving small animals. The device can operate off a single 3-V, 30-mAh coin cell battery for several weeks non-stop. To the best of the author's knowledge, the chip and miniaturized device presented in this work achieve the lowest power consumption among recently reported wireless FSCV systems. Last, a high-precision bidirectional-current potentiostat and a scalable CMOS VLSI electrochemical detector array incorporating the bidirectional potentiostat were developed for high-throughput amperometric and voltammetric recording of quantal release events, which is anticipated will accelerate the development and testing of new treatments that modulate the size and kinetics of quantal release.

5.2 Future Work

In this work, the microsystems developed for *in vivo* monitoring applications were validated *in vitro* with flow-injection analysis experiments. Future validation experiments for the wireless sensing microsystem certainly include performing preliminary *in vivo* monitoring studies with anesthetized rats as well as long-term behavioral studies with awake, freely-behaving rats. To accomplish this goal, additional circuitry for on-chip electrical stimulation and triangle waveform generation is expected. Increasing the number of channels will also enable parallel monitoring of different brain locations. Furthermore, addition of a receiver on-chip will allow bi-directional communication and real-time programmability of the device. Depending on the design of the receiver, operation in a wireless sensor network could be a possibility, which would enable long-term behavioral studies with multiple animals in the same environment. This experiment might be useful to gain more insight into the role of dopamine in social behavior.

Future validation experiments for the scalable array include further *in vitro* testing with flow-injection analysis and with cell cultures. To accomplish this goal, post-CMOS fabrication and surface-patterning of electrode material, in particular, deposition or electroplating of noble metals such as gold and platinum, is expected. Development of readout electronics to process the highly-multiplexed output data is also necessary. For real-time data transfer, a USB 3.0 protocol must be implemented for the host computer to be able to handle the high data rates in this application.

APPENDIX A

MINIATURIZED WIRELESS DEVICE: BOARD DESIGN

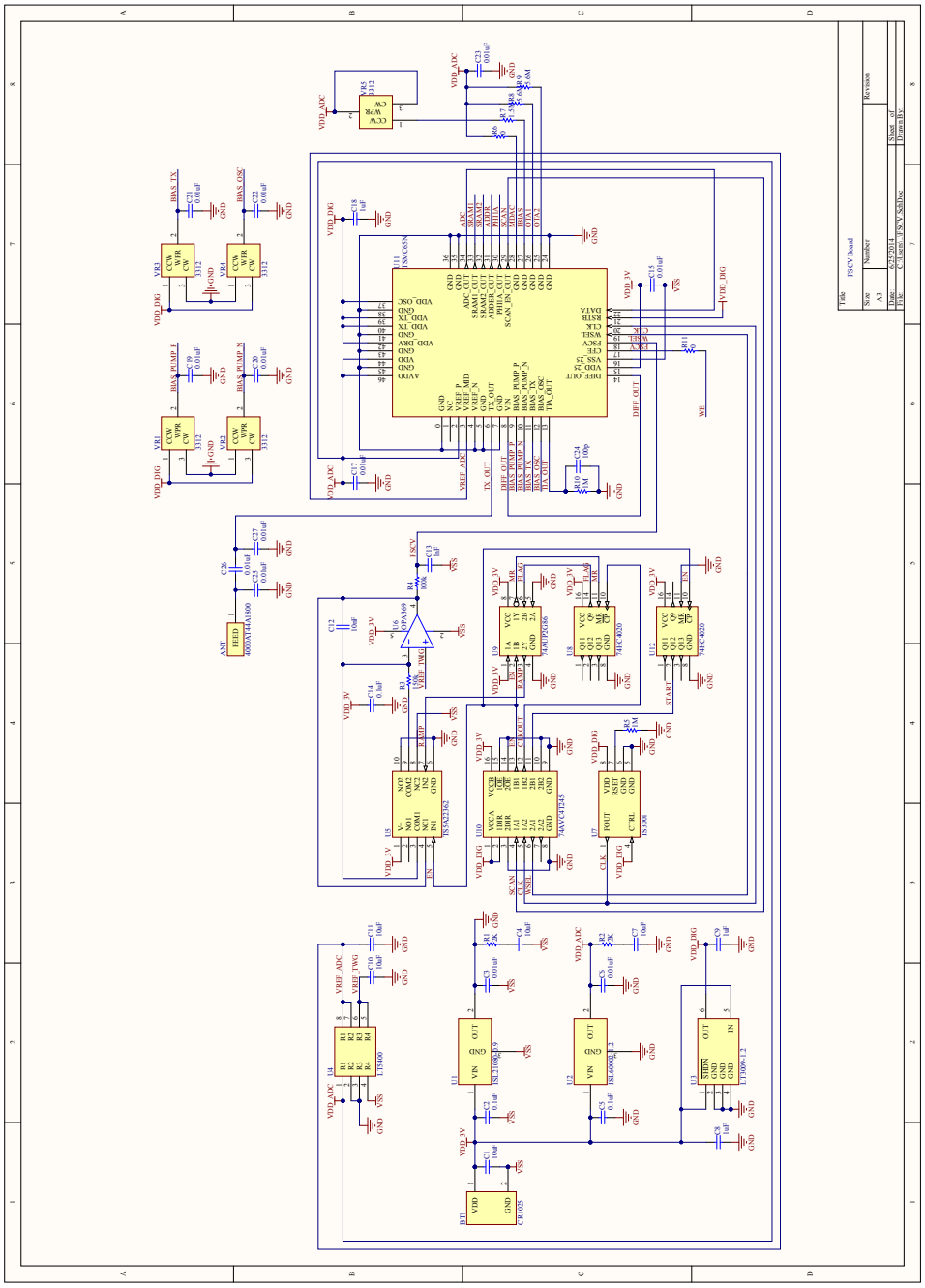

Figure A.1: Board schematic of the miniaturized wireless device in Ch. 3.

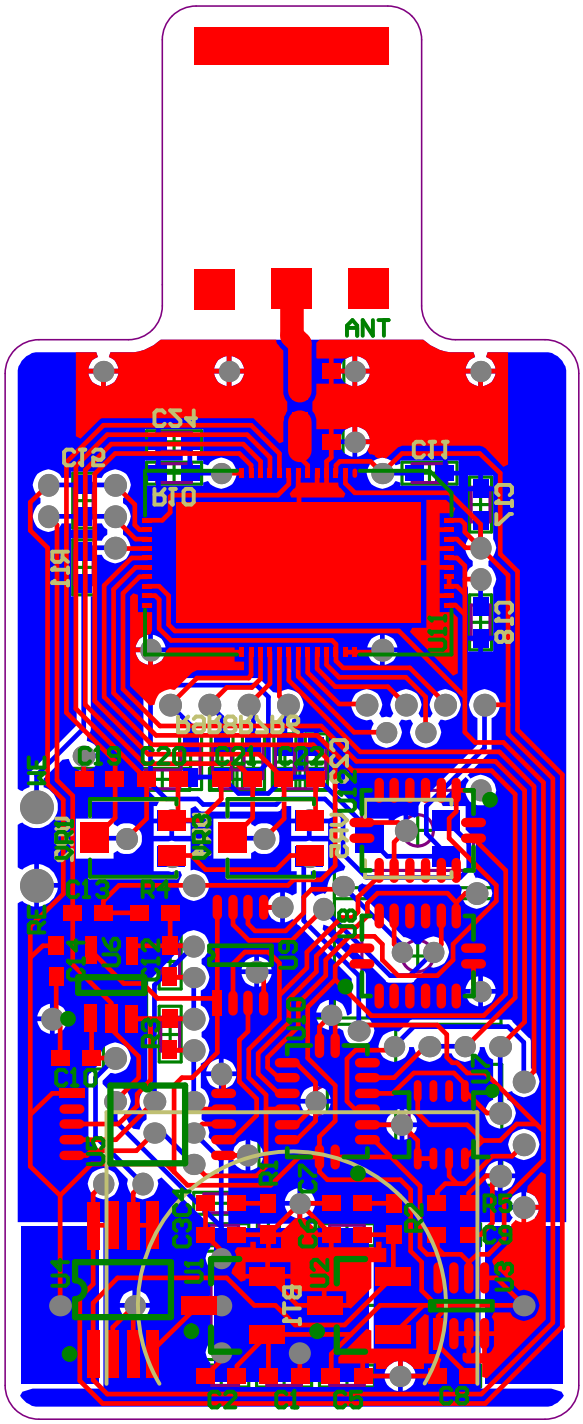

Figure A.2: Board layout of the miniaturized wireless device in Ch. 3.

Comment	Description	Designator	Footprint	LibRef	Quantity
4000AT44A1800	Johanson Technology UWB Antenna	ANT	ANT4000	4000AT44A1800	1
CR1025	Memory Protection Devices CR1025 Battery Holder	BT1	CR1025	CR1025	1
10uF	Capacitor (Semiconductor SIM Model)	C1, C4, C7, C10, C11	0402	Cap Semi	5
0.1uF	Capacitor (Semiconductor SIM Model)	C2, C5, C14	0402	Cap Semi	3
0.01uF	Capacitor (Semiconductor SIM Model)	C3, C6, C15, C17, C19, C20, C21, C22, C23, C25, C26, C27	0402	Cap Semi	12
1uF	Capacitor (Semiconductor SIM Model)	C8, C9, C18	0402	Cap Semi	3
10nF	Capacitor (Semiconductor SIM Model)	C12	0402	Cap Semi	1
1nF	Capacitor (Semiconductor SIM Model)	C13	0402	Cap Semi	1
100p	Capacitor (Semiconductor SIM Model)	C24	0402	Cap Semi	1
2K	Resistor	R1, R2	0402	Res1	2
150k	Resistor	R3	0402	Res1	1
100k	Resistor	R4	0402	Res1	1
1M	Resistor	R5, R10	0402	Res1	2
0	Resistor	R6, R11	0402	Res1	2
1.5M	Resistor	R7	0402	Res1	1
5.6M	Resistor	R8, R9	0402	Res1	2
ISL21080-0.9	Intersil Voltage Reference 0.9V	U1	SOT23_N	ISL21080	1
ISL60002-1.2	Intersil Voltage Reference 1.2V	U2	SOT23_N	ISL60002	1
LT3009-1.2	Linear Technology Low Dropout Regulator 1.2V	U3	SC70-8	LT3009	1
LT5400	Linear Technology Quad Matched Resistor Network	U4	MS8	LT5400	1
TS5A22362	Texas Instruments Dual SPDT Switches with Negative Signaling Capability	U5	VSSOP10	TS5A22362	1
OPA369	Enhanced Product, Micropower CMOS Operational Amplifier Zero-Drift Series, 1.8 to 5.5 V, -55 to 125 degC, 5-pin SOT23 (DCK5), Green (RoHS & no Sb/Br)	U6	TI-DCK5_V	OPA333AMDCKREP	1
TS3001	Touchstone Semiconductor Oscillator/Timer 10kHz	U7	TDFN22	TS3001	1
74HC4020	NXP Semiconductors 14-Stage Binary Ripple Counter	U8, U12	VFQFN16	74HC4020	2
74AUP2G86	NXP Semiconductors Dual 2-Input XOR Gate	U9	VSSOP8	74AUP2G86	1
74AVC4T245	NXP Semiconductors 2-Bit Dual-Supply Voltage Level Translator	U10	VFQFN16	74AVC4T245	1
TSMC65N	TSMC 65nm ASIC	U11	LCC46_0610	TSMC65N	1
3312	SMD Trimming Potentiome	VR1, VR2, VR3, VR4, VR	3312	3312	5

Figure A.3: Bill of materials for the miniaturized wireless device in Ch. 3.

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